STM32F401xB STM32F401xC

ARM Cortex-M4 32b MCU+FPU, 105 DMIPS, 256KB Flash/64KB RAM, 10 TIMs, 1 ADC, 11 comm. interfaces

Data brief

WLCSP49
(3 x 3 mm)

LQFP100 (14 × 14 mm)
LQFP64 (10 × 10 mm)

UFQFPN48
(7 × 7 mm)
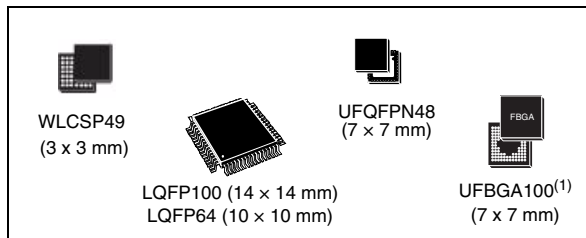
UFBGA100[1]
(7 x 7 mm)

1. UFBGA100 will be available soon.

Features

- Core: ARM 32-bit Cortex™-M4 CPU with FPU, Adaptive real-time accelerator (ART Accelerator™) allowing 0-wait state execution from Flash memory, frequency up to 84 MHz, memory protection unit, 105 DMIPS/ 1.25 DMIPS/MHz (Dhrystone 2.1), and DSP instructions

- Memories
  - Up to 256 Kbytes of Flash memory
  - Up to 64 Kbytes of SRAM

- Clock, reset and supply management
  - 1.7 V (PDR OFF) or 1.8 V (PDR ON) to 3.6 V application supply and I/Os
  - POR, PDR, PVD and BOR
  - 4-to-26 MHz crystal oscillator
  - Internal 16 MHz factory-trimmed RC
  - 32 kHz oscillator for RTC with calibration
  - Internal 32 kHz RC with calibration

- Power consumption
  - Run: 137 µA/MHz (peripheral off)
  - Stop (Flash in Stop mode, fast wakeup time): 50 µA typ @ 25 °C; 80 µA max @25 °C
  - Stop (Flash in Deep power down mode): down to 11 µA typ@ 25 °C; 40 µA max @25 °C
  - Standby: 2.4 µA @25 °C / 1.7 V without RTC; 12 µA @85 °C @1.7 V
  - V_{BAT} supply for RTC: 1 µA @25 °C

- 1×12-bit, 2.4 MSPS A/D converter: up to 16 channels

- General-purpose DMA: 16-stream DMA controllers with FIFOs and burst support

- Up to 10 timers: up to six 16-bit, two 32-bit timers up to 84 MHz, each with up to 4 IC/OC/PWM or pulse counter and quadrature (incremental) encoder input, two watchdog timers (independent and window)

- Debug mode
  - Serial wire debug (SWD) & JTAG interfaces
  - Cortex-M4 Embedded Trace Macrocell™

- Up to 79 I/O ports with interrupt capability
  - All IO ports 5 V tolerant
  - Up to 76 fast I/Os up to 42 MHz

- Up to 11 communication interfaces
  - Up to 3 × I²C interfaces (SMBus/PMBus)
  - Up to 3 USARTs (2 x 10.5 Mbit/s, 1 x 5.25 Mbit/s), ISO 7816 interface, LIN, IrDA, modem control)
  - Up to 4 SPIs (up to 42 Mbits/s at f_{CPU} = 84 MHz), SPI2 and SPI3 with muxed full-duplex I²S to achieve audio class accuracy via internal audio PLL or external clock
  - SDIO interface

- Advanced connectivity
  - USB 2.0 full-speed device/host/OTG controller with on-chip PHY

- CRC calculation unit

- 96-bit unique ID

- RTC: subsecond accuracy, hardware calendar

Table 1. Device summary

Reference	Part number
STM32F401xB	STM32F401CB, STM32F401RB, STM32F401VB
STM32F401xC	STM32F401CC, STM32F401RC, STM32F401VC

www.st.com

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1   Introduction

This databrief provides the description of the STM32F401xx line of microcontrollers.

The STM32F401xx data brief should be read in conjunction with the *STM32F40xxx, STM32F41xxx, STM32F42xxx, STM32F43xxx* reference manual RM0344.

The reference manual is available from the STMicroelectronics website *www.st.com*. It includes all information concerning Flash memory programming.

For information on the Cortex™-M4 core, please refer to the Cortex™-M4 programming manual (PM0214) available from www.st.com.

2   Description

The STM32F401xx device family is based on the high-performance ARM® Cortex™-M4 32-bit RISC core operating at a frequency of up to 84 MHz. Its Cortex-M4 with FPU core features a Floating point unit (FPU) single precision which supports all ARM single-precision data-processing instructions and data types. It also implements a full set of DSP instructions and a memory protection unit (MPU) which enhances application security.

STM32F401xx devices incorporate high-speed embedded memories (Flash memory up to 256 Kbytes, up to 64 Kbytes of SRAM), and up to 79 enhanced I/Os and peripherals connected to two APB buses, two AHB buses and a 32-bit multi-AHB bus matrix.

All devices offer one 12-bit ADC, a low-power RTC, six general-purpose 16-bit timers including one PWM timer for motor control, two general-purpose 32-bit timers. They also feature standard and advanced communication interfaces.

- Up to three I^{2}Cs
- Up to four SPIs
- Two full duplex I ^{2}S peripherals. To achieve audio class accuracy, the I^{2}S peripherals can be clocked via a dedicated internal audio PLL or via an external clock to allow synchronization.
- Three USARTs
- SDIO interface
- USB 2.0 OTG full speed interface

Refer to *Table 2: STM32F401xx features and peripheral counts* for the peripherals available for each part number.

The STM32F401xx devices operate in the –40 to +105 °C temperature range from a 1.7 (PDR OFF) to 3.6 V power supply. A comprehensive set of power-saving mode allows the design of low-power applications.

These features make the STM32F401xx microcontrollers suitable for a wide range of applications:

- Motor drive and application control
- Medical equipment
- Industrial applications: PLC, inverters, circuit breakers
- Printers, and scanners
- Alarm systems, video intercom, and HVAC
- Home audio appliances
- Mobile phone sensor hub

Figure 1 shows the general block diagram of the device family.

Table 2. STM32F401xx features and peripheral counts

Peripherals		STM32F401xB			STM32F401xC		
Flash memory in Kbytes		128			256		
SRAM in Kbytes	System	64					
Timers	General-purpose	7					
	Advanced-control	1					
Communication interfaces	SPI/ I^2S	3/2 (full duplex)		4/2 (full duplex)	3/2 (full duplex)		4/2 (full duplex)
	I^2C	3					
	USART	3					
	SDIO	-	1		-	1	
USB OTG FS		1					
GPIOs		36	50	81	36	50	81
12-bit ADC		1					
Number of channels		10	16		10	16	
Maximum CPU frequency		84 MHz					
Operating voltage		1.7 to 3.6 V					
Operating temperatures		Ambient temperatures: –40 to +85 °C/–40 to +105 °C					
		Junction temperature: –40 to + 125 °C					
Package		WLCSP49 UFQFPN48	LQFP64	LQFP100	WLCSP49 UFQFPN48	LQFP64	LQFP100

Figure 1. STM32F401xx block diagram
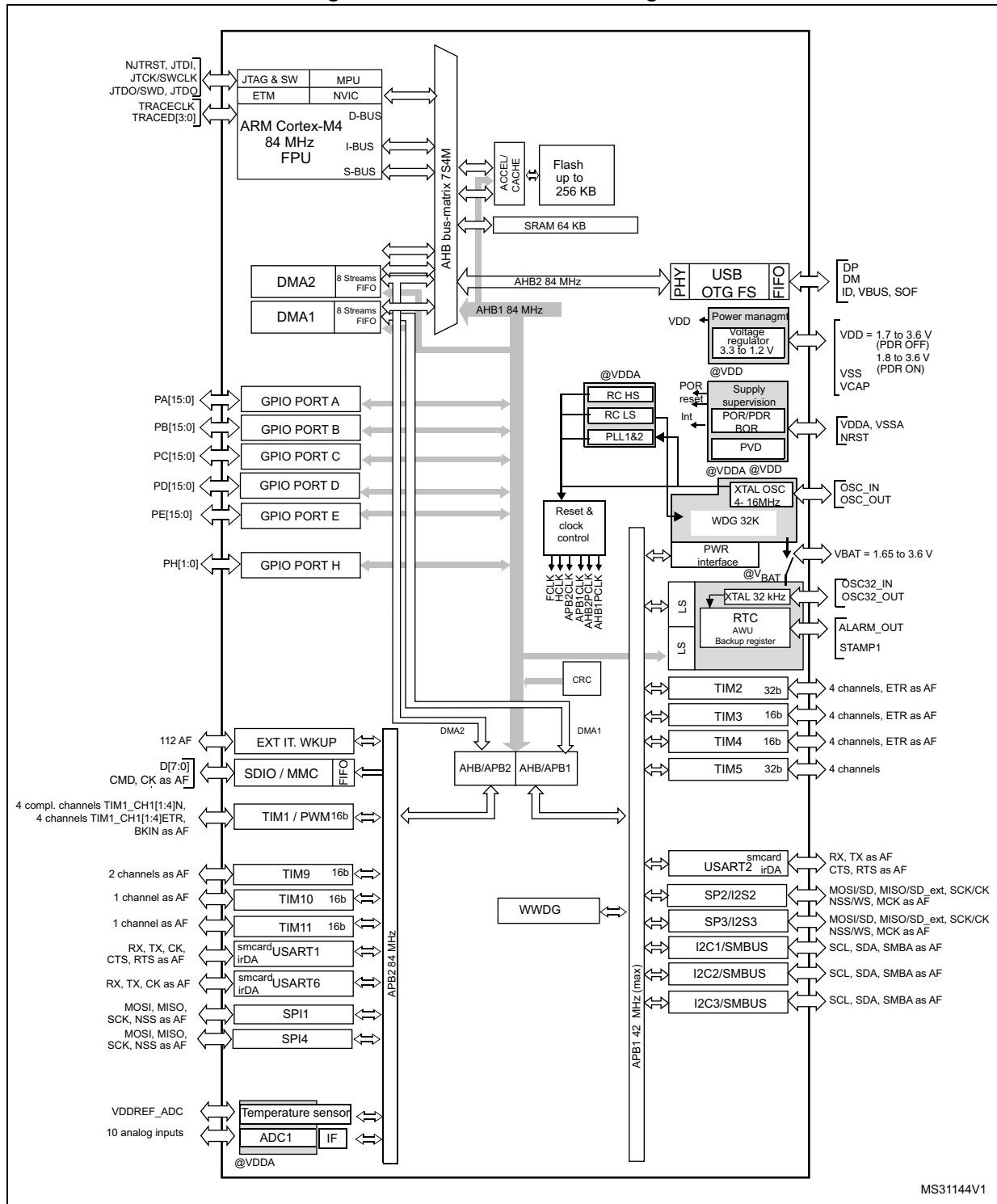
1. The timers connected to APB2 are clocked from TIMxCLK up to 84 MHz, while the timers connected to APB1 are clocked from TIMxCLK up to 42 MHz.

3 Functional overview

3.1 ARM® Cortex™-M4 with FPU core with embedded Flash and SRAM

The ARM Cortex-M4 with FPU processor is the latest generation of ARM processors for embedded systems. It was developed to provide a low-cost platform that meets the needs of MCU implementation, with a reduced pin count and low-power consumption, while delivering outstanding computational performance and an advanced response to interrupts.

The ARM Cortex-M4 with FPU 32-bit RISC processor features exceptional code-efficiency, delivering the high-performance expected from an ARM core in the memory size usually associated with 8- and 16-bit devices.

The processor supports a set of DSP instructions which allow efficient signal processing and complex algorithm execution.

Its single precision FPU (floating point unit) speeds up software development by using metalanguage development tools, while avoiding saturation.

The STM32F401xx family is compatible with all ARM tools and software.

Figure 1 shows the general block diagram of the STM32F401xx family.

Note: *Cortex-M4 with FPU is binary compatible with Cortex-M3.*

3.2 Adaptive real-time memory accelerator (ART Accelerator™)

The ART Accelerator™ is a memory accelerator which is optimized for STM32 industry-standard ARM® Cortex™-M4 with FPU processors. It balances the inherent performance advantage of the ARM Cortex-M4 with FPU over Flash memory technologies, which normally requires the processor to wait for the Flash memory at higher frequencies.

To release the processor full 105 DMIPS performance at this frequency, the accelerator implements an instruction prefetch queue and branch cache, which increases program execution speed from the 128-bit Flash memory. Based on CoreMark benchmark, the performance achieved thanks to the ART accelerator is equivalent to 0 wait state program execution from Flash memory at a CPU frequency up to 84 MHz.

3.3 Memory protection unit

The memory protection unit (MPU) is used to manage the CPU accesses to memory to prevent one task to accidentally corrupt the memory or resources used by any other active task. This memory area is organized into up to 8 protected areas that can in turn be divided up into 8 subareas. The protection area sizes are between 32 bytes and the whole 4 gigabytes of addressable memory.

The MPU is especially helpful for applications where some critical or certified code has to be protected against the misbehavior of other tasks. It is usually managed by an RTOS (real-time operating system). If a program accesses a memory location that is prohibited by the MPU, the RTOS can detect it and take action. In an RTOS environment, the kernel can dynamically update the MPU area setting, based on the process to be executed.

The MPU is optional and can be bypassed for applications that do not need it.

3.4   Embedded Flash memory

The devices embed a Flash memory of up to 256 Kbytes available for storing programs and data.

3.5   CRC (cyclic redundancy check) calculation unit

The CRC (cyclic redundancy check) calculation unit is used to get a CRC code from a 32-bit data word and a fixed generator polynomial.

Among other applications, CRC-based techniques are used to verify data transmission or storage integrity. In the scope of the EN/IEC 60335-1 standard, they offer a means of verifying the Flash memory integrity. The CRC calculation unit helps compute a software signature during runtime, to be compared with a reference signature generated at link-time and stored at a given memory location.

3.6   Embedded SRAM

All devices embed:

- Up to 64 Kbytes of system SRAM

    RAM memory is accessed (read/write) at CPU clock speed with 0 wait states

3.7 Multi-AHB bus matrix

The 32-bit multi-AHB bus matrix interconnects all the masters (CPU, DMAs) and the slaves (Flash memory, RAM, AHB and APB peripherals) and ensures a seamless and efficient operation even when several high-speed peripherals work simultaneously.

Figure 2. Multi-AHB matrix
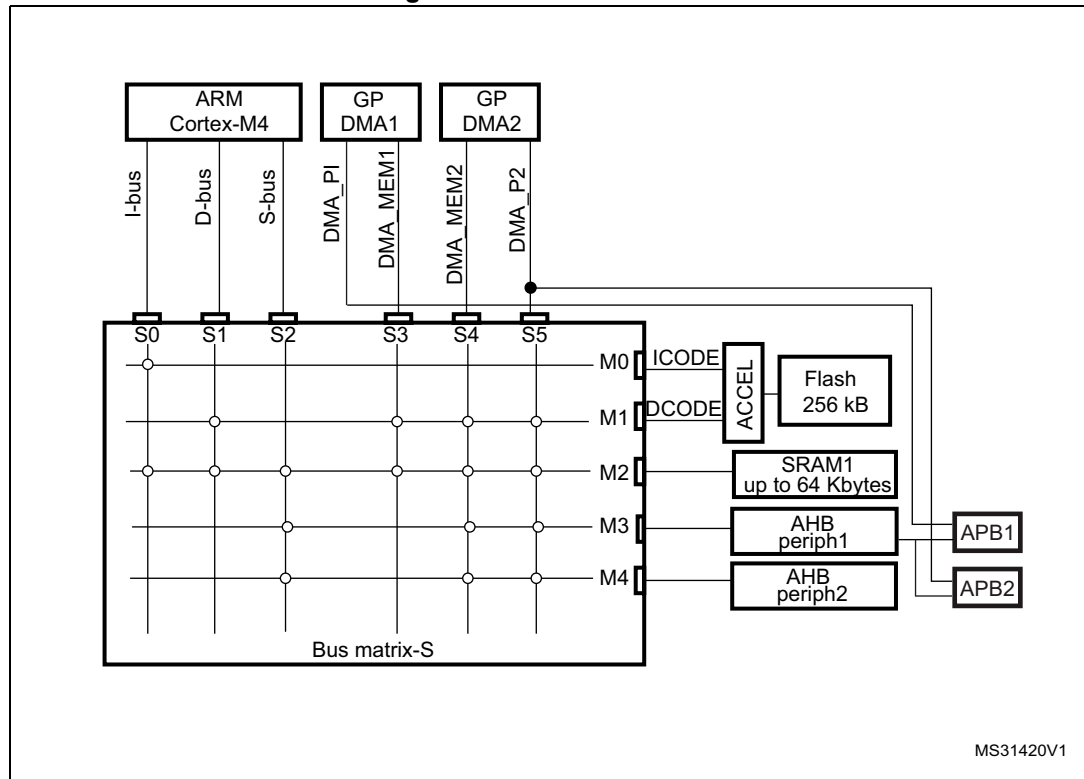
3.8 DMA controller (DMA)

The devices feature two general-purpose dual-port DMAs (DMA1 and DMA2) with 8 streams each. They are able to manage memory-to-memory, peripheral-to-memory and memory-to-peripheral transfers. They feature dedicated FIFOs for APB/AHB peripherals, support burst transfer and are designed to provide the maximum peripheral bandwidth (AHB/APB).

The two DMA controllers support circular buffer management, so that no specific code is needed when the controller reaches the end of the buffer. The two DMA controllers also have a double buffering feature, which automates the use and switching of two memory buffers without requiring any special code.

Each stream is connected to dedicated hardware DMA requests, with support for software trigger on each stream. Configuration is made by software and transfer sizes between source and destination are independent.

The DMA can be used with the main peripherals:

- SPI and I^{2}S
- I^{2}C
- USART
- General-purpose, basic and advanced-control timers TIMx
- ADC

3.9 Nested vectored interrupt controller (NVIC)

The devices embed a nested vectored interrupt controller able to manage 16 priority levels, and handle up to 62 maskable interrupt channels plus the 16 interrupt lines of the Cortex™-M4 with FPU.

- Closely coupled NVIC gives low-latency interrupt processing
- Interrupt entry vector table address passed directly to the core
- Allows early processing of interrupts
- Processing of late arriving, higher-priority interrupts
- Support tail chaining
- Processor state automatically saved
- Interrupt entry restored on interrupt exit with no instruction overhead

This hardware block provides flexible interrupt management features with minimum interrupt latency.

3.10 External interrupt/event controller (EXTI)

The external interrupt/event controller consists of 23 edge-detector lines used to generate interrupt/event requests. Each line can be independently configured to select the trigger event (rising edge, falling edge, both) and can be masked independently. A pending register maintains the status of the interrupt requests. The EXTI can detect an external line with a pulse width shorter than the Internal APB2 clock period. Up to 81 GPIOs can be connected to the 16 external interrupt lines.

3.11 Clocks and startup

On reset the 16 MHz internal RC oscillator is selected as the default CPU clock. The 16 MHz internal RC oscillator is factory-trimmed to offer 1% accuracy at 25 °C. The application can then select as system clock either the RC oscillator or an external 4-26 MHz clock source. This clock can be monitored for failure. If a failure is detected, the system automatically switches back to the internal RC oscillator and a software interrupt is generated (if enabled). This clock source is input to a PLL thus allowing to increase the frequency up to 84 MHz. Similarly, full interrupt management of the PLL clock entry is available when necessary (for example if an indirectly used external oscillator fails).

Several prescalers allow the configuration of the two AHB buses, the high-speed APB (APB2) and the low-speed APB (APB1) domains. The maximum frequency of the two AHB buses is 84 MHz while the maximum frequency of the high-speed APB domains is 84 MHz. The maximum allowed frequency of the low-speed APB domain is 42 MHz.

The devices embed a dedicated PLL (PLLI2S) which allows to achieve audio class performance. In this case, the I^{2}S master clock can generate all standard sampling frequencies from 8 kHz to 192 kHz.

3.12 Boot modes

At startup, boot pins are used to select one out of three boot options:

- Boot from user Flash
- Boot from system memory
- Boot from embedded SRAM

The boot loader is located in system memory. It is used to reprogram the Flash memory by using USART1 (PA9/PA10).

3.13 Power supply schemes

- V_{DD} = 1.7 to 3.6 V: external power supply for I/Os with the internal regulator disabled, provided externally through V_{DD} pins. Requires the use of an external power supply supervisor connected to the VDD and PDR_ON pins.
- V_{DD} = 1.8 to 3.6 V: external power supply for I/Os and the internal regulator (when enabled), provided externally through V_{DD} pins.
- V_{SSA}, V_{DDA} = 1.8 to 3.6 V: external analog power supplies for ADC, Reset blocks, RCs and PLL. V_{DDA} and V_{SSA} must be connected to V_{DD} and V_{SS}, respectively, with decoupling technique.
- V_{BAT} = 1.65 to 3.6 V: power supply for RTC, external clock 32 kHz oscillator and backup registers (through power switch) when V_{DD} is not present.

3.14 Power supply supervisor

Internal power supply supervisor enabled

This feature is available for V_{DD} operating voltage range 1.8 V to 3.6 V

The internal power supply supervisor is enabled by holding PDR_ON high.

The device has an integrated power-on reset (POR)/ power-down reset (PDR) circuitry coupled with a Brownout reset (BOR) circuitry. At power-on, POR is always active, and ensures proper operation starting from 1.8 V. After the 1.8 V POR threshold level is reached, the option byte loading process starts, either to confirm or modify default thresholds, or to disable BOR permanently. Three BOR thresholds are available through option bytes.
The device remains in reset mode when V_{DD} is below a specified threshold, $V_{POR/PDR}$ or V_{BOR}, without the need for an external reset circuit.

The device also features an embedded programmable voltage detector (PVD) that monitors the V_{DD}/V_{DDA} power supply and compares it to the V_{PVD} threshold. An interrupt can be generated when V_{DD}/V_{DDA} drops below the V_{PVD} threshold and/or when V_{DD}/V_{DDA} is higher than the V_{PVD} threshold. The interrupt service routine can then generate a warning message and/or put the MCU into a safe state. The PVD is enabled by software.

The device has an internal reset controlled through the PDR_ON signal.

3.14.1 Internal reset OFF

This feature is available only on packages featuring the PDR_ON pin. The internal power-on reset (POR) / power-down reset (PDR) circuitry is disabled through the PDR_ON pin.

An external power supply supervisor should monitor V_{DD} and should maintain the device in reset mode as long as V_{DD} is below a specified threshold. PDR_ON should be connected to this external power supply supervisor. Refer to *Figure 3: Power supply supervisor interconnection with internal reset OFF*.

Figure 3. Power supply supervisor interconnection with internal reset OFF
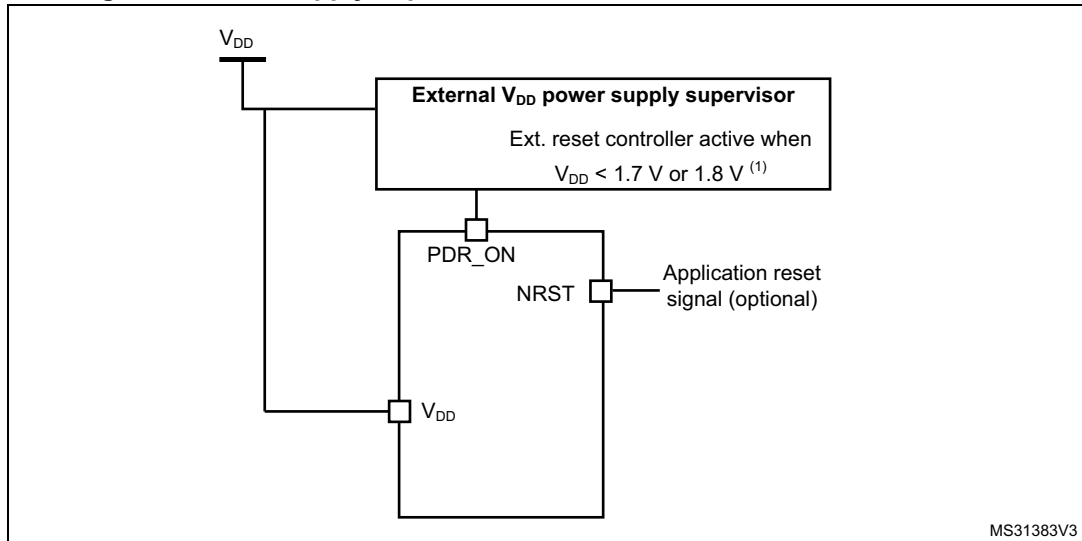
1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

The V_{DD} specified threshold, below which the device must be maintained under reset, is 1.8 V (see *Figure 4*). This supply voltage can drop to 1.7 V when the device operates in the 0 to 70 °C temperature range.

A comprehensive set of power-saving mode allows to design low-power applications.

When the internal reset is OFF, the following integrated features are no more supported:

- The integrated power-on reset (POR) / power-down reset (PDR) circuitry is disabled
- The brownout reset (BOR) circuitry must be disabled
- The embedded programmable voltage detector (PVD) is disabled
- V_{BAT} functionality is no more available and V_{BAT} pin should be connected to V_{DD}.

Figure 4. PDR_ON control with internal reset OFF
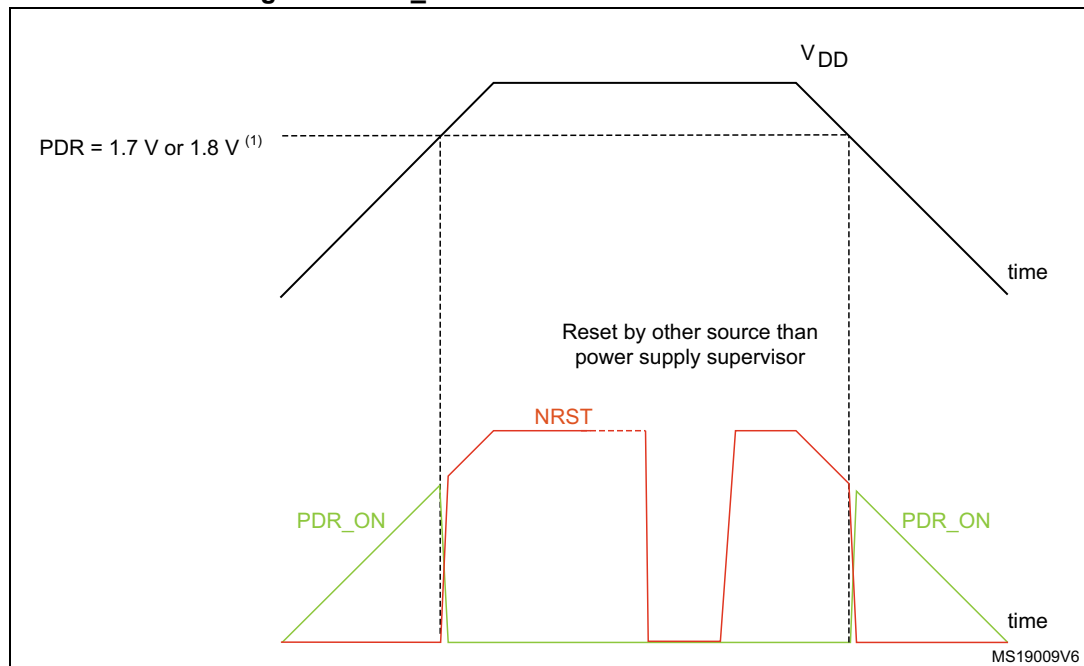
1. PDR = 1.7 V for reduce temperature range; PDR = 1.8 V for all temperature range.

3.14.2 Voltage regulator

The regulator has four operating modes:

- Regulator ON
  - Main regulator mode (MR)
  - Low power regulator (LPR)
  - Power-down
- Regulator OFF

3.14.3 Regulator ON

On packages embedding the BYPASS_REG pin, the regulator is enabled by holding BYPASS_REG low. On all other packages, the regulator is always enabled.

There are three power modes configured by software when the regulator is ON:

- MR is used in the nominal regulation mode (With different voltage scaling in Run)

  In Main regulator mode (MR mode), different voltage scaling are provided to reach the best compromise between maximum frequency and dynamic power consumption.

- LPR is used in the Stop modes

  The LP regulator mode is configured by software when entering Stop mode.

- Power-down is used in Standby mode.

  The Power-down mode is activated only when entering in Standby mode. The regulator output is in high impedance and the kernel circuitry is powered down, inducing zero consumption. The contents of the registers and SRAM are lost)

Two external ceramic capacitors should be connected on V_{CAP_1} and V_{CAP_2} pin.

All packages have the regulator ON feature.

3.14.4 Regulator OFF

This feature is available only on packages featuring the BYPASS_REG pin. The regulator is disabled by holding BYPASS_REG high. The regulator OFF mode allows to supply externally a V12 voltage source through V_{CAP_1} and V_{CAP_2} pins.

Since the internal voltage scaling is not managed internally, the external voltage value must be aligned with the targeted maximum frequency.

The two V_{CAP} ceramic capacitors should be replaced by two 100 nF decoupling capacitors.

When the regulator is OFF, there is no more internal monitoring on V12. An external power supply supervisor should be used to monitor the V12 of the logic power domain. PA0 pin should be used for this purpose, and act as power-on reset on V12 power domain.

In regulator OFF mode, the following features are no more supported:

- PA0 cannot be used as a GPIO pin since it allows to reset a part of the V12 logic power domain which is not reset by the NRST pin.
- As long as PA0 is kept low, the debug mode cannot be used under power-on reset. As a consequence, PA0 and NRST pins must be managed separately if the debug connection under reset or pre-reset is required.

The following conditions must be respected:

- V_{DD} should always be higher than V_{CAP_1} and V_{CAP_2} to avoid current injection between power domains.
- If the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is faster than the time for V_{DD} to reach 1.8 V, then PA0 should be kept low to cover both conditions: until V_{CAP_1} and V_{CAP_2} reach V_{12} minimum value and until V_{DD} reaches V12 1.8 V (see *Figure 5*).
- Otherwise, if the time for V_{CAP_1} and V_{CAP_2} to reach V_{12} minimum value is slower than the time for V_{DD} to reach 1.8 V, then PA0 could be asserted low externally (see *Figure 6*).
- If V_{CAP_1} and V_{CAP_2} go below V_{12} minimum value and V_{DD} is higher than 1.8 V, then a reset must be asserted on PA0 pin.

Note: The minimum value of V_{12} depends on the maximum frequency targeted in the application

**Figure 5. Startup in regulator OFF: slow V_{DD} slope
- power-down reset risen after V_{CAP_1}/V_{CAP_2} stabilization**
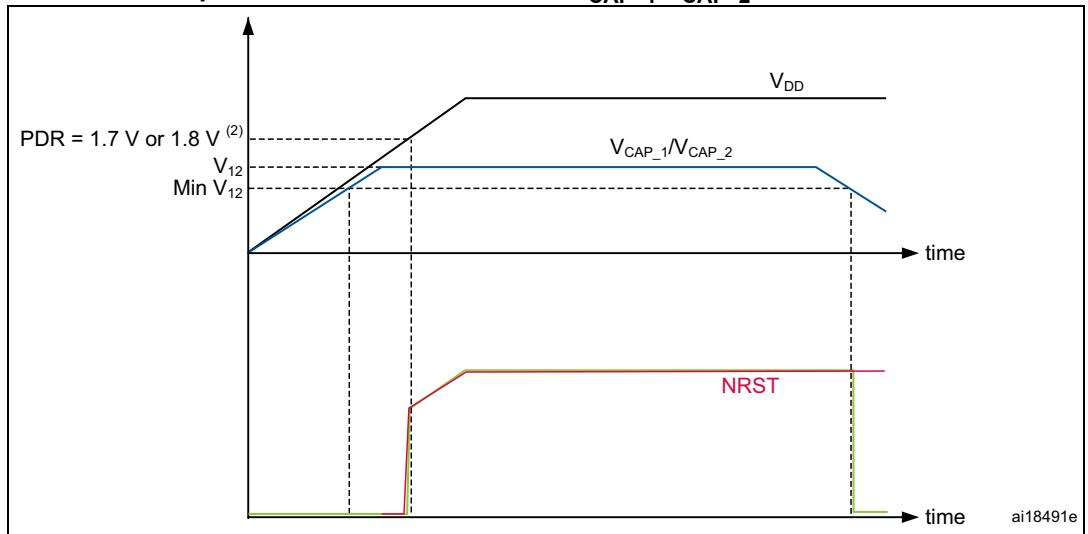
1. This figure is valid whatever the internal reset mode (ON or OFF).
2. PDR = 1.7 V for a reduced temperature range; PDR = 1.8 V for all temperature ranges.

**Figure 6. Startup in regulator OFF mode: fast V_{DD} slope
- power-down reset risen before V_{CAP_1}/V_{CAP_2} stabilization**
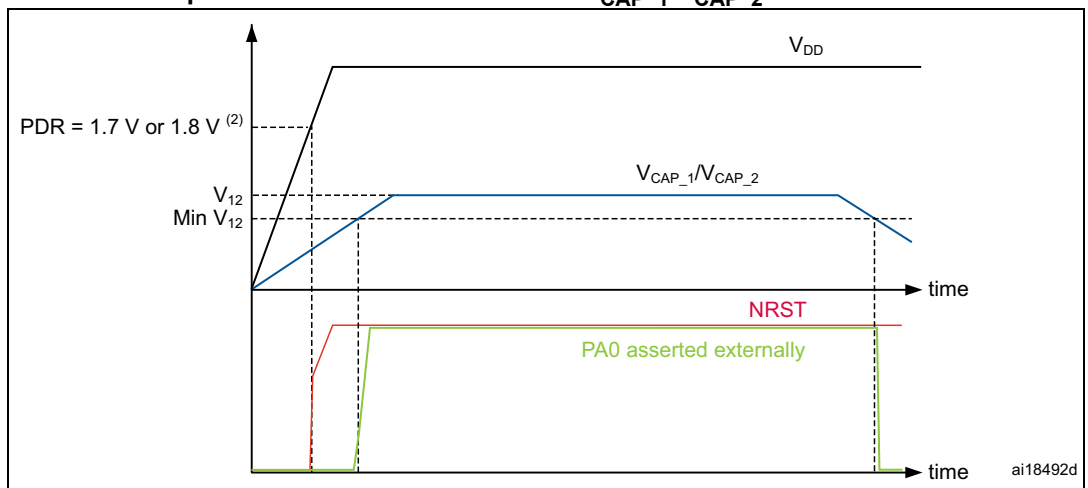
1. This figure is valid whatever the internal reset mode (ON or OFF).
2. PDR = 1.7 V for a reduced temperature range; PDR = 1.8 V for all temperature ranges.

3.14.5 Regulator ON/OFF and internal power supply supervisor availability

Table 3. Regulator ON/OFF and internal power supply supervisor availability

Package	Regulator ON	Regulator OFF	Power supply supervisor ON	Power supply supervisor OFF
UFQFPN48	Yes	No	Yes	Yes
WLCSP49	Yes	No	Yes PDR_ON set to VDD	Yes PDR_ON external control[1]
LQFP64	Yes	No	Yes	No
LQFP100	Yes	No	Yes	No

1. Refer to *Section 3.14: Power supply supervisor*

3.15 Real-time clock (RTC) and backup registers

The backup domain includes:

- The real-time clock (RTC)
- 20 backup registers

The real-time clock (RTC) is an independent BCD timer/counter. Dedicated registers contain the second, minute, hour (in 12/24 hour), week day, date, month, year, in BCD (binary-coded decimal) format. Correction for 28, 29 (leap year), 30, and 31 day of the month are performed automatically. The RTC provides a programmable alarm and programmable periodic interrupts with wakeup from Stop and Standby modes. The sub-seconds value is also available in binary format.

It is clocked by a 32.768 kHz external crystal, resonator or oscillator, the internal low-power RC oscillator or the high-speed external clock divided by 128. The internal low-speed RC has a typical frequency of 32 kHz. The RTC can be calibrated using an external 512 Hz output to compensate for any natural quartz deviation.

Two alarm registers are used to generate an alarm at a specific time and calendar fields can be independently masked for alarm comparison. To generate a periodic interrupt, a 16-bit programmable binary auto-reload downcounter with programmable resolution is available and allows automatic wakeup and periodic alarms from every 120 µs to every 36 hours.

A 20-bit prescaler is used for the time base clock. It is by default configured to generate a time base of 1 second from a clock at 32.768 kHz.

The backup registers are 32-bit registers used to store 80 bytes of user application data when V_{DD} power is not present. Backup registers are not reset by a system, a power reset, or when the device wakes up from the Standby mode (see *Section 3.16: Low-power modes*).

Additional 32-bit registers contain the programmable alarm subseconds, seconds, minutes, hours, day, and date.

The RTC and backup registers are supplied through a switch that is powered either from the V_{DD} supply when present or from the V_{BAT} pin.

3.16 Low-power modes

The devices support three low-power modes to achieve the best compromise between low power consumption, short startup time and available wakeup sources:

- **Sleep mode**

  In Sleep mode, only the CPU is stopped. All peripherals continue to operate and can wake up the CPU when an interrupt/event occurs.

- **Stop mode**

  The Stop mode achieves the lowest power consumption while retaining the contents of SRAM and registers. All clocks in the 1.2 V domain are stopped, the PLL, the HSI RC

and the HSE crystal oscillators are disabled. The voltage regulator can also be put either in normal or in low-power mode.

The device can be woken up from the Stop mode by any of the EXTI line (the EXTI line source can be one of the 16 external lines, the PVD output, the RTC alarm/ wakeup/ tamper/ time stamp events).

- **Standby mode**

  The Standby mode is used to achieve the lowest power consumption. The internal voltage regulator is switched off so that the entire 1.2 V domain is powered off. The PLL, the HSI RC and the HSE crystal oscillators are also switched off. After entering Standby mode, the SRAM and register contents are lost except for registers in the backup domain when selected.

  The device exits the Standby mode when an external reset (NRST pin), an IWDG reset, a rising edge on the WKUP pin, or an RTC alarm/ wakeup/ tamper/time stamp event occurs.

  The standby mode is not supported when the embedded voltage regulator is bypassed and the 1.2 V domain is controlled by an external power.

Note: *When in Standby mode, only an RTC alarm/event or an external reset can wake up the device provided V_{DD} is supplied by an external battery.*

3.17 V_{BAT} operation

The V_{BAT} pin allows to power the device V_{BAT} domain from an external battery, an external supercapacitor, or from V_{DD} when no external battery and an external supercapacitor are present.

V_{BAT} operation is activated when V_{DD} is not present.

The V_{BAT} pin supplies the RTC and the backup registers.

Note: *When the microcontroller is supplied from V_{BAT}, external interrupts and RTC alarm/events do not exit it from V_{BAT} operation.*

3.18 Timers and watchdogs

The devices include one advanced-control timer, seven general-purpose timers and two watchdog timers.

All timer counters can be frozen in debug mode.

Table 4 compares the features of the advanced-control and general-purpose timers.

Table 4. Timer feature comparison

Timer type	Timer	Counter resolution	Counter type	Prescaler factor	DMA request generation	Capture/ compare channels	Complementary output	Max interface clock (MHz)	Max timer clock (MHz)
Advanced-control	TIM1	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	Yes	84	84
General purpose	TIM2, TIM5	32-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM3, TIM4	16-bit	Up, Down, Up/down	Any integer between 1 and 65536	Yes	4	No	42	84
	TIM9	16-bit	Up	Any integer between 1 and 65536	No	2	No	84	84
	TIM10, TIM11	16-bit	Up	Any integer between 1 and 65536	No	1	No	84	84

3.18.1 Advanced-control timers (TIM1)

The advanced-control timer (TIM1) can be seen as three-phase PWM generators multiplexed on 4 independent channels. It has complementary PWM outputs with programmable inserted dead times. It can also be considered as a complete general-purpose timer. Its 4 independent channels can be used for:

- Input capture
- Output compare
- PWM generation (edge- or center-aligned modes)
- One-pulse mode output

If configured as standard 16-bit timers, it has the same features as the general-purpose TIMx timers. If configured as a 16-bit PWM generator, it has full modulation capability (0-100%).

The advanced-control timer can work together with the TIMx timers via the Timer Link feature for synchronization or event chaining.

TIM1 supports independent DMA request generation.

3.18.2 General-purpose timers (TIMx)

There are seven synchronizable general-purpose timers embedded in the STM32F401xx devices (see *Table 4* for differences).

- **TIM2, TIM3, TIM4, TIM5**

  The STM32F401xx include 4 full-featured general-purpose timers: TIM2, TIM5, TIM3, and TIM4.The TIM2 and TIM5 timers are based on a 32-bit auto-reload up/downcounter and a 16-bit prescaler. The TIM3 and TIM4 timers are based on a 16-bit auto-reload up/downcounter and a 16-bit prescaler. They all feature 4 independent channels for input capture/output compare, PWM or one-pulse mode output. This gives up to 16 input capture/output compare/PWMs on the largest packages.

  The TIM2, TIM3, TIM4, TIM5 general-purpose timers can work together, or with the other general-purpose timers and the advanced-control timers TIM1 and TIM8 via the Timer Link feature for synchronization or event chaining.

  Any of these general-purpose timers can be used to generate PWM outputs.

  TIM2, TIM3, TIM4, TIM5 all have independent DMA request generation. They are capable of handling quadrature (incremental) encoder signals and the digital outputs from 1 to 4 hall-effect sensors.

- **TIM9, TIM10 and TIM11**

  These timers are based on a 16-bit auto-reload upcounter and a 16-bit prescaler. TIM10 and TIM11 feature one independent channel, whereas TIM9 has two independent channels for input capture/output compare, PWM or one-pulse mode output. They can be synchronized with the TIM2, TIM3, TIM4, TIM5 full-featured general-purpose timers. They can also be used as simple time bases.

3.18.3 Independent watchdog

The independent watchdog is based on a 12-bit downcounter and 8-bit prescaler. It is clocked from an independent 32 kHz internal RC and as it operates independently from the main clock, it can operate in Stop and Standby modes. It can be used either as a watchdog to reset the device when a problem occurs, or as a free-running timer for application timeout management. It is hardware- or software-configurable through the option bytes.

3.18.4 Window watchdog

The window watchdog is based on a 7-bit downcounter that can be set as free-running. It can be used as a watchdog to reset the device when a problem occurs. It is clocked from the main clock. It has an early warning interrupt capability and the counter can be frozen in debug mode.

3.18.5 SysTick timer

This timer is dedicated to real-time operating systems, but could also be used as a standard downcounter. It features:

- A 24-bit downcounter
- Autoreload capability
- Maskable system interrupt generation when the counter reaches 0
- Programmable clock source.

3.19 Inter-integrated circuit interface (I²C)

Up to three I²C bus interfaces can operate in multimaster and slave modes. They can support the Standard- and Fast-modes. Fast mode plus at 1 MHz is also possible and is described in a separate application note. They support the 7/10-bit addressing mode and the 7-bit dual addressing mode (as slave). A hardware CRC generation/verification is embedded.

They can be served by DMA and they support SMBus 2.0/PMBus.

The devices also include programmable analog and digital noise filters (see *Table 5*).

Table 5. Comparison of I2C analog and digital filters

	Analog filter	Digital filter
Pulse width of suppressed spikes	≥ 50 ns	Programmable length from 1 to 15 I2C peripheral clocks
Benefits	Available in Stop mode	1. Extra filtering capability vs. standard requirements. 2. Stable length
Drawbacks	Variations depending on temperature, voltage, process	Disabled when Wakeup from Stop mode is enabled

3.20 Universal synchronous/asynchronous receiver transmitters (USART)

The devices embed three universal synchronous/asynchronous receiver transmitters (USART1, USART2 and USART6).

These three interfaces provide asynchronous communication, IrDA SIR ENDEC support, multiprocessor communication mode, single-wire half-duplex communication mode and have LIN Master/Slave capability. The USART1 and USART6 interfaces are able to communicate at speeds of up to 10.5 Mbit/s. The USART2 interface communicates at up to 5.25 bit/s.

USART1 and USART2 also provide hardware management of the CTS and RTS signals, Smart Card mode (ISO 7816 compliant) and SPI-like communication capability. All interfaces can be served by the DMA controller.

Table 6. USART feature comparison

USART name	Standard features	Modem (RTS/CTS)	LIN	SPI master	irDA	Smartcard (ISO 7816)	Max. baud rate in Mbit/s (oversampling by 16)	Max. baud rate in Mbit/s (oversampling by 8)	APB mapping
USART1	X	X	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)
USART2	X	X	X	X	X	X	2.62	5.25	APB1 (max. 42 MHz)
USART6	X	N.A	X	X	X	X	5.25	10.5	APB2 (max. 84 MHz)

3.21 Serial peripheral interface (SPI)

The devices feature up to four SPIs in slave and master modes in full-duplex and simplex communication modes. SPI1 and SPI4 can communicate at up to 42 Mbits/s, SPI2 and SPI3 can communicate at up to 21 Mbit/s. The 3-bit prescaler gives 8 master mode frequencies and the frame is configurable to 8 bits or 16 bits. The hardware CRC generation/verification supports basic SD Card/MMC modes. All SPIs can be served by the DMA controller.

The SPI interface can be configured to operate in TI mode for communications in master mode and slave mode.

3.22 Inter-integrated sound (I^2S)

Two standard I^2S interfaces (multiplexed with SPI2 and SPI3) are available. They can be operated in master or slave mode, in full duplex and simplex communication modes, and can be configured to operate with a 16-/32-bit resolution as an input or output channel. Audio sampling frequencies from 8 kHz up to 192 kHz are supported. When either or both of the I^2S interfaces is/are configured in master mode, the master clock can be output to the external DAC/CODEC at 256 times the sampling frequency.

All I^2Sx can be served by the DMA controller.

3.23 Audio PLL (PLLI2S)

The devices feature an additional dedicated PLL for audio I^2S application. It allows to achieve error-free I^2S sampling clock accuracy without compromising on the CPU performance.

The PLLI2S configuration can be modified to manage an I^2S sample rate change without disabling the main PLL (PLL) used for the CPU.

The audio PLL can be programmed with very low error to obtain sampling rates ranging from 8 KHz to 192 KHz.

In addition to the audio PLL, a master clock input pin can be used to synchronize the I2S flow with an external PLL (or Codec output).

3.24 Secure digital input/output interface (SDIO)

An SD/SDIO/MMC host interface is available, that supports MultiMediaCard System Specification Version 4.2 in three different databus modes: 1-bit (default), 4-bit and 8-bit.

The interface allows data transfer at up to 48 MHz, and is compliant with the SD Memory Card Specification Version 2.0.

The SDIO Card Specification Version 2.0 is also supported with two different databus modes: 1-bit (default) and 4-bit.

The current version supports only one SD/SDIO/MMC4.2 card at any one time and a stack of MMC4.1 or previous.

In addition to SD/SDIO/MMC, this interface is fully compliant with the CE-ATA digital protocol Rev1.1.

3.25 Universal serial bus on-the-go full-speed (OTG_FS)

The devices embed an USB OTG full-speed device/host/OTG peripheral with integrated transceivers. The USB OTG FS peripheral is compliant with the USB 2.0 specification and with the OTG 1.0 specification. It has software-configurable endpoint setting and supports suspend/resume. The USB OTG full-speed controller requires a dedicated 48 MHz clock that is generated by a PLL connected to the HSE oscillator. The major features are:

- Combined Rx and Tx FIFO size of 320 × 35 bits with dynamic FIFO sizing
- Supports the session request protocol (SRP) and host negotiation protocol (HNP)
- 4 bidirectional endpoints
- 8 host channels with periodic OUT support
- HNP/SNP/IP inside (no need for any external resistor)
- For OTG/Host modes, a power switch is needed in case bus-powered devices are connected

3.26 General-purpose input/outputs (GPIOs)

Each of the GPIO pins can be configured by software as output (push-pull or open-drain, with or without pull-up or pull-down), as input (floating, with or without pull-up or pull-down) or as peripheral alternate function. Most of the GPIO pins are shared with digital or analog alternate functions. All GPIOs are high-current-capable and have speed selection to better manage internal noise, power consumption and electromagnetic emission.

The I/O configuration can be locked if needed by following a specific sequence in order to avoid spurious writing to the I/Os registers.

Fast I/O handling allowing maximum I/O toggling up to 84 MHz.

3.27   Analog-to-digital converter (ADC)

One 12-bit analog-to-digital converter is embedded and shares up to 16 external channels, performing conversions in the single-shot or scan mode. In scan mode, automatic conversion is performed on a selected group of analog inputs.

Additional logic functions embedded in the ADC interface allow:

*   Simultaneous sample and hold
*   Interleaved sample and hold

The ADC can be served by the DMA controller. An analog watchdog feature allows very precise monitoring of the converted voltage of one, some or all selected channels. An interrupt is generated when the converted voltage is outside the programmed thresholds.

To synchronize A/D conversion and timers, the ADCs could be triggered by any of TIM1, TIM2, TIM3, TIM4 or TIM5 timer.

3.28   Temperature sensor

The temperature sensor has to generate a voltage that varies linearly with temperature. The conversion range is between 1.7 V and 3.6 V. The temperature sensor is internally connected to the ADC_IN18 input channel which is used to convert the sensor output voltage into a digital value.

As the offset of the temperature sensor varies from chip to chip due to process variation, the internal temperature sensor is mainly suitable for applications that detect temperature changes instead of absolute temperatures. If an accurate temperature reading is needed, then an external temperature sensor part should be used.

3.29   Serial wire JTAG debug port (SWJ-DP)

The ARM SWJ-DP interface is embedded, and is a combined JTAG and serial wire debug port that enables either a serial wire debug or a JTAG probe to be connected to the target.

Debug is performed using 2 pins only instead of 5 required by the JTAG (JTAG pins could be re-use as GPIO with alternate function): the JTAG TMS and TCK pins are shared with SWDIO and SWCLK, respectively, and a specific sequence on the TMS pin is used to switch between JTAG-DP and SW-DP.

3.30   Embedded Trace Macrocell™

The ARM Embedded Trace Macrocell provides a greater visibility of the instruction and data flow inside the CPU core by streaming compressed data at a very high rate from the STM32F401xx through a small number of ETM pins to an external hardware trace port analyzer (TPA) device. The TPA is connected to a host computer using any high-speed channel available. Real-time instruction and data flow activity can be recorded and then formatted for display on the host computer that runs the debugger software. TPA hardware is commercially available from common development tool vendors.

The Embedded Trace Macrocell operates with third party debugger software tools.

4 Pinouts and pin description

Table 7. STM32F401xx WLCSP49 pinout[1]

	7	6	5	4	3	2	1
A	VDD	VSS	BOOT0	PB4	PB3	PA15	PA14
B	VBAT	PDR_ON	PB8	PB5	PA13	VDD	VSS
C	PC14	PC15	PB9	PB6	PA12	PA10	PA11
D	PH0	PH1	PC13	PB7	VSS	PA9	PA8
E	NRST	VSSA VREF-	PA2	PA3	PB10	PB12	PB15
F	VDDA VREF+	PA0	PA5	PA6	PA7	VDD	PB14
G	PA1	PA4	PB0	PB1	PB2	VCAP1	PB13

1. The above figure shows the package bottom view.

Figure 7. STM32F401xx UFQFPN48 pinout
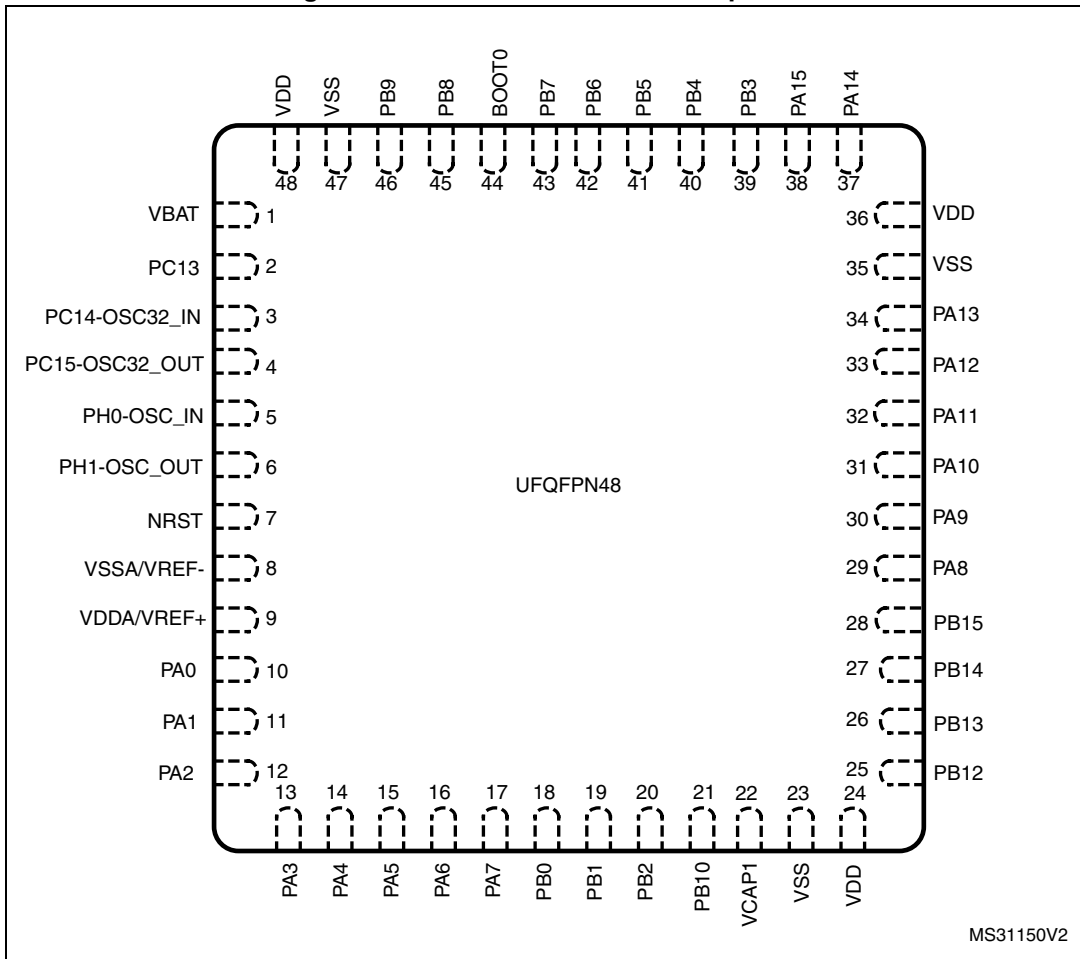
1. The above figure shows the package top view.

Figure 8. STM32F401xx LQFP64 pinout
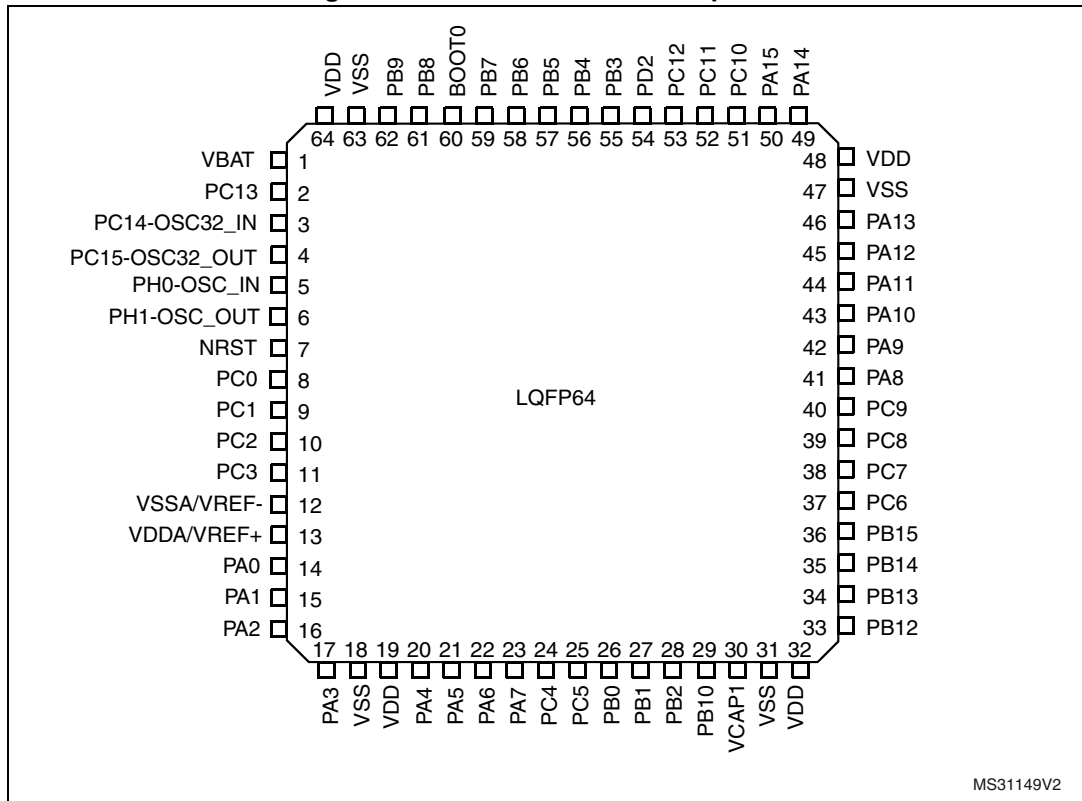
1. The above figure shows the package top view.

Figure 9. STM32F401xx LQFP100 pinout
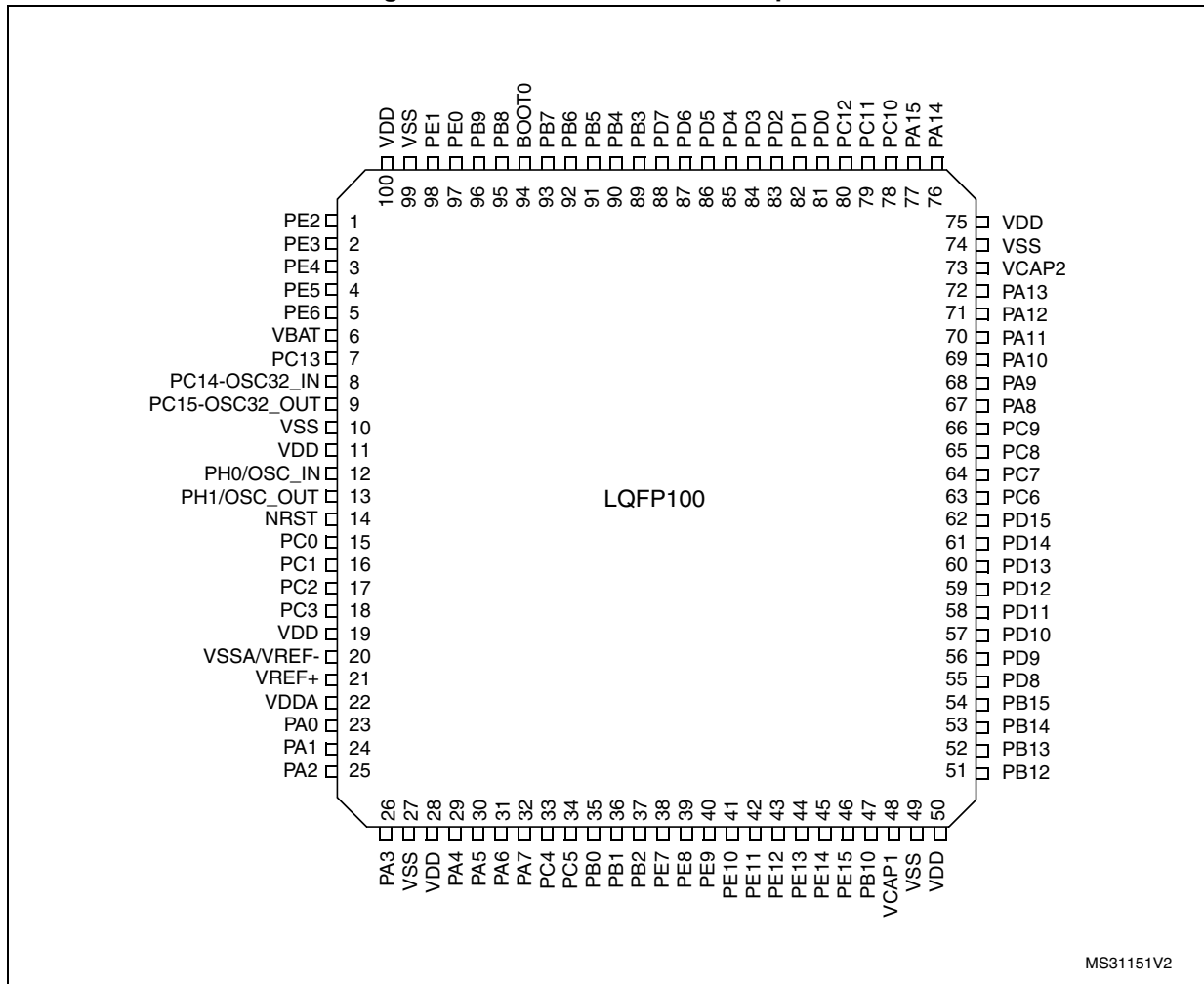
1.   The above figure shows the package top view.

Table 8. Legend/abbreviations used in the pinout table

Name	Abbreviation	Definition
Pin name		Unless otherwise specified in brackets below the pin name, the pin function during and after reset is the same as the actual pin name
Pin type	S	Supply pin
	I	Input only pin
	I/O	Input/ output pin
I/O structure	FT	5 V tolerant I/O
	B	Dedicated BOOT0 pin
	NRST	Bidirectional reset pin with embedded weak pull-up resistor
Notes		Unless otherwise specified by a note, all I/Os are set as floating inputs during and after reset

Table 8. Legend/abbreviations used in the pinout table (continued)

Name	Abbreviation	Definition
Alternate functions		Functions selected through GPIOx_AFR registers
Additional functions		Functions directly selected/enabled through peripheral registers

Table 9. STM32F401xx pin definitions

UQFN48	LQFP64	LQFP100	WLCSP49	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	-	1	-	PE2				SPI4_SCK, TRACECLK	
-	-	2	-	PE3				TRACED0	
-	-	3	-	PE4				SPI4_NSS, TRACED1	
-	-	4	-	PE5				SPI4_MISO, TIM9_CH1, TRACED2	
-	-	5	-	PE6				SPI4_MOSI, TIM9_CH2, TRACED3	
1	1	6	B7	VBAT					
2	2	7	D5	PC13-ANTI_TAMP					TAMP_1
3	3	8	C7	PC14-OSC32_IN					OSC32_IN
4	4	9	C6	PC15-OSC32_OUT					OSC32_OUT
-	-	10	-	VSS					
-	-	11	-	VDD					
5	5	12	D7	PH0 - OSC_IN					OSC_IN
6	6	13	D6	PH1 - OSC_OUT					OSC_OUT
7	7	14	E7	NRST					
-	8	15	-	PC0					ADC1_10

Table 9. STM32F401xx pin definitions (continued)

UQFN48	LQFP64	LQFP100	WLCSP49	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
-	9	16	-	PC1					ADC1_11
-	10	17	-	PC2				SPI2_MISO, I2S2ext_SD	ADC1_12
-	11	18	-	PC3				SPI2_MOSI/I2S2_SD	ADC1_13
-	-	19	-	VDD					
8	12	20	E6	VSSA/VREF-					
9	13	-	-	VDDA/VREF+					
-	-	21	-	VREF+					
-	-	22	F7	VDDA					
10	14	23	F6	PA0-WKUP				USART2_CTS, TIM2_CH1/TIM2_ETR, TIM5_CH1	ADC1_0, WKUP
11	15	24	G7	PA1				USART2_RTS, TIM2_CH2, TIM5_CH2	ADC1_1
12	16	25	E5	PA2				USART2_TX, TIM2_CH3, TIM5_CH3, TIM9_CH1	ADC1_2
13	17	26	E4	PA3				USART2_RX, TIM2_CH4, TIM5_CH4, TIM9_CH2	ADC1_3
-	18	27	-	VSS					
-	19	28	-	VDD					
14	20	29	G6	PA4				SPI1_NSS, SPI3_NSS/I2S3_WS, USART2_CK	ADC1_4
15	21	30	F5	PA5				SPI1_SCK, TIM2_CH1/TIM2_ETR	ADC1_5
16	22	31	F4	PA6				SPI1_MISO, TIM1_BKIN, TIM3_CH1	ADC1_6
17	23	32	F3	PA7				SPI1_MOSI, TIM1_CH1N, TIM3_CH2	ADC1_7
-	24	33	-	PC4					ADC1_14
-	25	34	-	PC5					ADC1_15

Table 9. STM32F401xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	LQFP64	LQFP100	WLCSP49						
18	26	35	G5	PB0				TIM1_CH2N, TIM3_CH3	ADC1_8
19	27	36	G4	PB1				TIM1_CH3N, TIM3_CH4	ADC1_9
20	28	37	G3	PB2					
-	-	38	-	PE7				TIM1_ETR	
-	-	39	-	PE8				TIM1_CH1N	
-	-	40	-	PE9				TIM1_CH1	
-	-	41	-	PE10				TIM1_CH2N	
-	-	42	-	PE11				SPI4_NSS, TIM1_CH2	
-	-	43	-	PE12				SPI4_SCK, TIM1_CH3N	
-	-	44	-	PE13				SPI4_MISO, TIM1_CH3	
-	-	45	-	PE14				SPI4_MOSI, TIM1_CH4	
-	-	46	-	PE15				TIM1_BKIN	
21	29	47	E3	PB10				SPI2_SCK/I2S2_CK, I2C2_SCL, TIM2_CH3	
22	30	48	G2	VCAP1					
23	31	49	D3	VSS					
24	32	50	F2	VDD					
25	33	51	E2	PB12				SPI2_NSS/I2S2_WS, I2C2_SMBAL, TIM1_BKIN	
26	34	52	G1	PB13				SPI2_SCK/I2S2_CK, TIM1_CH1N	
27	35	53	F1	PB14				SPI2_MISO, I2S2ext_SD, TIM1_CH2N	
28	36	54	E1	PB15				SPI2_MOSI/I2S2_SD, TIM1_CH3N, RTC_50Hz	
-	-	55	-	PD8					
-	-	56	-	PD9					
-	-	57	-	PD10					

Table 9. STM32F401xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	LQFP64	LQFP100	WLCSP49						
-	-	58	-	PD11					
-	-	59	-	PD12				TIM4_CH1	
-	-	60	-	PD13				TIM4_CH2	
-	-	61	-	PD14				TIM4_CH3	
-	-	62	-	PD15				TIM4_CH4	
-	37	63	-	PC6				I2S2_MCK, USART6_TX, TIM3_CH1, SDIO_D6	
-	38	64	-	PC7				I2S3_MCK, USART6_RX, TIM3_CH2, SDIO_D7	
-	39	65	-	PC8				USART6_CK, TIM3_CH3, SDIO_D0	
-	40	66	-	PC9				I2S2_CKIN, I2C3_SDA, TIM3_CH4, SDIO_D1, MCO_2	
29	41	67	D1	PA8				I2C3_SCL, USART1_CK, TIM1_CH1, USB_FS_SOF, MCO_1	
30	42	68	D2	PA9				I2C3_SMBAL, USART1_TX, TIM1_CH2, USB_FS_VBUS	
31	43	69	C2	PA10				USART1_RX, TIM1_CH3, USB_FS_ID	
32	44	70	C1	PA11				USART1_CTS, USART6_TX, TIM1_CH4, USB_FS_DM	
33	45	71	C3	PA12				USART1_RTS, USART6_RX, TIM1_ETR, USB_FS_DP	
34	46	72	B3	PA13				JTMS-SWDIO	
-	-	73	-	VCAP2					
35	47	74	B1	VSS					
36	48	75	-	VDD					
-	-	-	B2	VDD					
37	49	76	A1	PA14				JTCK-SWCLK	

Table 9. STM32F401xx pin definitions (continued)

Pin Number				Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
UQFN48	LQFP64	LQFP100	WLCSP49						
38	50	77	A2	PA15				SPI1_NSS, SPI3_NSS/I2S3_WS, TIM2_CH1/TIM2_ETR, JTDI	
-	51	78	-	PC10				SPI3_SCK/I2S3_CK, SDIO_D2	
-	52	79	-	PC11				I2S3ext_SD, SPI3_MISO, SDIO_D3	
-	53	80	-	PC12				SPI3_MOSI/I2S3_SD, SDIO_CK	
-	-	81	-	PD0					
-	-	82	-	PD1					
-	54	83	-	PD2				TIM3_ETR, SDIO_CMD	
-	-	84	-	PD3				SPI2_SCK/I2S2_CK, USART2_CTS	
-	-	85	-	PD4				USART2_RTS	
-	-	86	-	PD5				USART2_TX	
-	-	87	-	PD6				SPI3_MOSI/I2S3_SD, USART2_RX	
-	-	88	-	PD7				USART2_CK	
39	55	89	A3	PB3				SPI1_SCK, SPI3_SCK/I2S3_CK, I2C2_SDA, TIM2_CH2, JTDO-SWO	
40	56	90	A4	PB4				SPI1_MISO, SPI3_MISO, I2S3ext_SD, I2C3_SDA, TIM3_CH1, JTRST	
41	57	91	B4	PB5				SPI1_MOSI, SPI3_MOSI/I2S3_SD, I2C1_SMBAL, TIM3_CH2	
42	58	92	C4	PB6				I2C1_SCL, USART1_TX, TIM4_CH1	
43	59	93	D4	PB7				I2C1_SDA, USART1_RX, TIM4_CH2	

Table 9. STM32F401xx pin definitions (continued)

UQFN48	LQFP64	LQFP100	WLCSP49	Pin name (function after reset)	Pin type	I/O structure	Notes	Alternate functions	Additional functions
44	60	94	A5	BOOT0					
45	61	95	B5	PB8				I2C1_SCL, TIM4_CH3, TIM10_CH1, SDIO_D4	
46	62	96	C5	PB9				SPI2_NSS/I2S2_WS, I2C1_SDA, TIM4_CH4, TIM11_CH1, SDIO_D5	
-	-	97	-	PE0				TIM4_ETR	
-	-	98	-	PE1					
47	63	99	A6	VSS					
-	-	-	B6	PDR_ON					
48	64	100	A7	VDD					

Table 10. Alternate function mapping

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_ FS		SDIO			
Port A	PA0		TIM2_CH1/TIM2_ETR	TIM5_CH1					USART2_CTS								
	PA1		TIM2_CH2	TIM5_CH2					USART2_RTS								
	PA2		TIM2_CH3	TIM5_CH3	TIM9_CH1				USART2_TX								
	PA3		TIM2_CH4	TIM5_CH4	TIM9_CH2				USART2_RX								
	PA4						SPI1_NSS	SPI3_NSS/I2S3_WS	USART2_CK								
	PA5		TIM2_CH1/TIM2_ETR				SPI1_SCK										
	PA6		TIM1_BKIN	TIM3_CH1			SPI1_MISO										
	PA7		TIM1_CH1N	TIM3_CH2			SPI1_MOSI										
	PA8	MCO_1	TIM1_CH1			I2C3_SCL			USART1_CK			USB_FS_SOF					
	PA9		TIM1_CH2			I2C3_SMBAL			USART1_TX			USB_FS_VBUS					
	PA10		TIM1_CH3						USART1_RX			USB_FS_ID					
	PA11		TIM1_CH4						USART1_CTS	USART6_TX		USB_FS_DM					
	PA12		TIM1_ETR						USART1_RTS	USART6_RX		USB_FS_DP					
	PA13	JTMS-SWDIO															
	PA14	JTCK-SWCLK															
	PA15	JTDI	TIM2_CH1/TIM2_ETR				SPI1_NSS	SPI3_NSS/I2S3_WS									

Table 10. Alternate function mapping (continued)

Port		AF00 SYS_AF	AF01 TIM1/TIM2	AF02 TIM3/ TIM4/ TIM5	AF03 TIM9/ TIM10/ TIM11	AF04 I2C1/I2C2/ I2C3	AF05 SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	AF06 SPI2/I2S2/ SPI3/ I2S3	AF07 SPI3/I2S3/ USART1/ USART2	AF08 USART6	AF09 I2C2/ I2C3	AF10 OTG1_ FS	AF11	AF12 SDIO	AF13	AF14	AF15
Port B	PB0		TIM1_CH2N	TIM3_CH3													
	PB1		TIM1_CH3N	TIM3_CH4													
	PB2																
	PB3	JTDO-SWO	TIM2_CH2				SPI1_SCK	SPI3_SCK/I2S3_CK			I2C2_SDA						
	PB4	JTRST		TIM3_CH1			SPI1_MISO	SPI3_MISO	I2S3ext_SD		I2C3_SDA						
	PB5			TIM3_CH2		I2C1_SMBAL	SPI1_MOSI	SPI3_MOSI/I2S3_SD									
	PB6			TIM4_CH1		I2C1_SCL			USART1_TX								
	PB7			TIM4_CH2		I2C1_SDA			USART1_RX								
	PB8			TIM4_CH3	TIM10_CH1	I2C1_SCL								SDIO _D4			
	PB9			TIM4_CH4	TIM11_CH1	I2C1_SDA	SPI2_NSS/ I2S2_WS							SDIO _D5			
Port B	PB10		TIM2_CH3			I2C2_SCL	SPI2_SCK/ I2S2_CK										
	PB12		TIM1_BKIN			I2C2_SMBAL	SPI2_NSS/ I2S2_WS										
	PB13		TIM1_CH1N				SPI2_SCK/ I2S2_CK										
	PB14		TIM1_CH2N				SPI2_MISO	I2S2ext_SD									
	PB15	RTC_50Hz	TIM1_CH3N				SPI2_MOSI/ I2S2_SD										
Port C	PC0																

Table 10. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_ FS		SDIO			
Port C	PC1																
	PC2						SPI2_MISO	I2S2ext_SD									
	PC3						SPI2_MOSI/ I2S2_SD										
	PC4																
	PC5																
	PC6			TIM3_CH1			I2S2_MCK			USART6_TX				SDIO _D6			
	PC7			TIM3_CH2				I2S3_MCK		USART6_RX				SDIO _D7			
	PC8			TIM3_CH3						USART6_CK				SDIO _D0			
	PC9	MCO_2		TIM3_CH4		I2C3_SDA	I2S2_CKIN							SDIO _D1			
	PC10							SPI3_SCK/I2S3_ CK						SDIO _D2			
	PC11						I2S3ext_SD	SPI3_MISO						SDIO _D3			
	PC12							SPI3_MOSI/I2S3 _SD						SDIO _CK			
	PC13																
	PC14																
	PC15																

Table 10. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_ FS		SDIO			
Port D	PD0																
	PD1																
	PD2			TIM3_ETR										SDIO _CMD			
	PD3						SPI2_SCK/I2S2 _CK		USART2_CTS								
	PD4								USART2_RTS								
Port D	PD5								USART2_TX								
	PD6						SPI3_MOSI/ I2S3_SD		USART2_RX								
	PD7								USART2_CK								
	PD8																
	PD9																
	PD10																
	PD11																
	PD12			TIM4_CH1													
	PD13			TIM4_CH2													
	PD14			TIM4_CH3													
	PD15			TIM4_CH4													

Table 10. Alternate function mapping (continued)

Port		AF00	AF01	AF02	AF03	AF04	AF05	AF06	AF07	AF08	AF09	AF10	AF11	AF12	AF13	AF14	AF15
		SYS_AF	TIM1/TIM2	TIM3/ TIM4/ TIM5	TIM9/ TIM10/ TIM11	I2C1/I2C2/ I2C3	SPI1/SPI2/ I2S2/SPI3/ I2S3/SPI4	SPI2/I2S2/ SPI3/ I2S3	SPI3/I2S3/ USART1/ USART2	USART6	I2C2/ I2C3	OTG1_ FS		SDIO			
Port E	PE0			TIM4_ETR													
	PE1		TIM1_CH2N														
	PE2	TRACECLK					SPI4_SCK										
	PE3	TRACED0															
	PE4	TRACED1					SPI4_NSS										
	PE5	TRACED2			TIM9_CH1		SPI4_MISO										
	PE6	TRACED3			TIM9_CH2		SPI4_MOSI										
	PE7		TIM1_ETR														
	PE8		TIM1_CH1N														
	PE9		TIM1_CH1														
	PE10		TIM1_CH2N														
	PE11		TIM1_CH2				SPI4_NSS										
	PE12		TIM1_CH3N				SPI4_SCK										
	PE13		TIM1_CH3				SPI4_MISO										
	PE14		TIM1_CH4				SPI4_MOSI										
	PE15		TIM1_BKIN														
Port H	PH0																
	PH1																

5   Package characteristics

5.1   Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: *www.st.com*. ECOPACK® is an ST trademark.

5.1.1 WLCSP49 wafer level chip size package

Figure 10. WLCSP49 package dimensions (in mm)
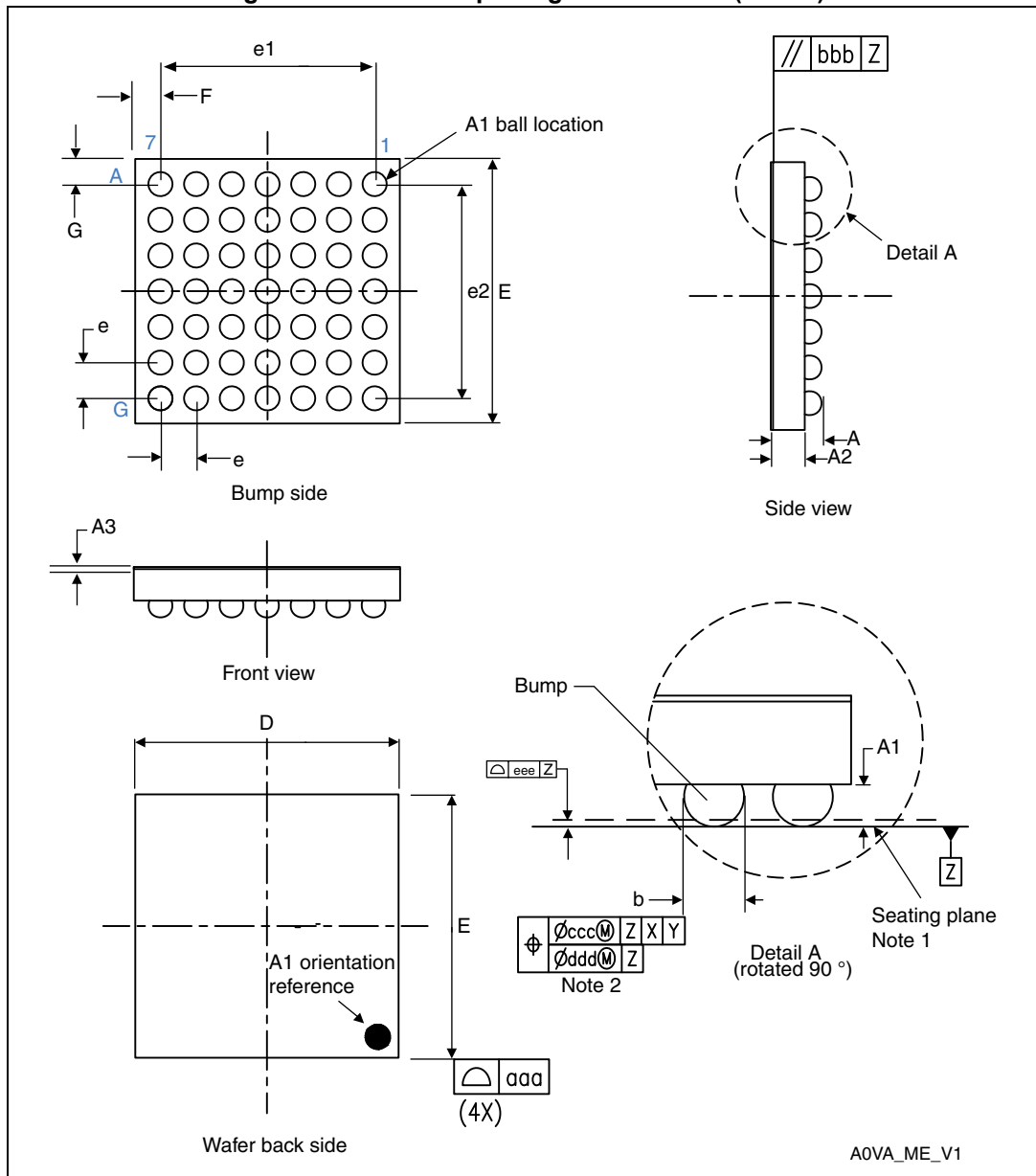
1. Primary datum Z and seating plane are defined by the spherical crowns of the bump.
2. Bump position designation per JESD 95-1, SPP-010.

Table 11. WLCSP49 wafer level chip size package mechanical data

Symbol	millimeters			inches[1]		
	Min	**Typ**	**Max**	**Min**	**Typ**	**Max**
A	0.525	0.555	0.585	0.0207	0.0219	0.0230
A1		0.175			0.0069	
A2		0.380			0.0150	
A3[2]		0.025			0.0010	
b[3]	0.220	0.250	0.280	0.0087	0.0098	0.0110
D	2.930	2.965	3.000	0.1154	0.1167	0.1181
E	2.930	2.965	3.000	0.1154	0.1167	0.1181
e		0.400			0.0157	
e1		2.400			0.0945	
e2		2.400			0.0945	
F		0.283			0.0111	
G		0.283			0.0111	
aaa		0.100			0.0039	
bbb		0.100			0.0039	
ccc		0.100			0.0039	
ddd		0.050			0.0020	
eee		0.050			0.0020	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

2. Back side coating

3. Dimension is measured at the maximum bump diameter parallel to primary datum Z.

Marking of engineering samples

The following figure shows the engineering sample marking for the WLCSP49 package. Only the information field containing the engineering sample marking is shown.

Figure 11. WLCSP49 package top view
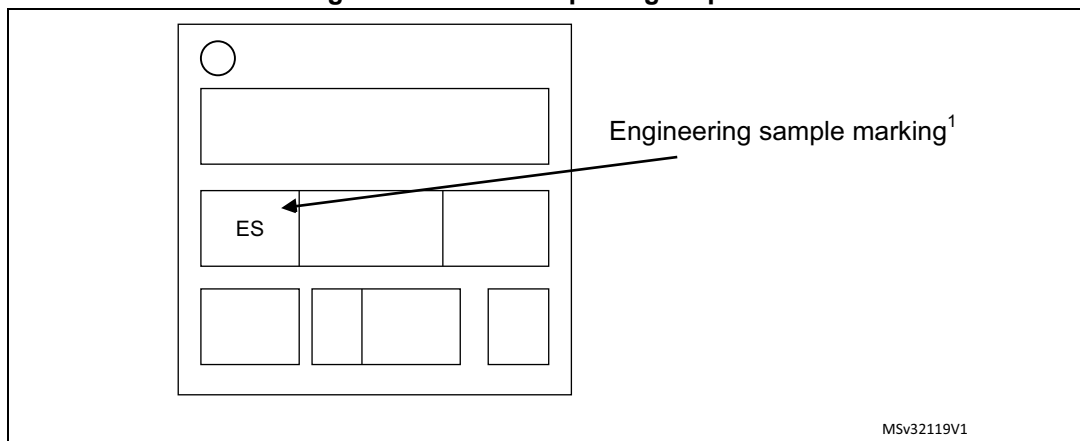
1. Devices identified with "ES" are engineering samples intended to be sent to the customer for electrical compatibility evaluation. They may be used to start customer qualification. Therefore, ST is not liable for any customer usage in production and/or in reliability qualification trials.

5.1.2 UFQFPN48 7 x 7 mm, 0.5 mm pitch package

Figure 12. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package outline[1][2][3]

Figure 13. Recommended footprint (dimensions in mm)[1]
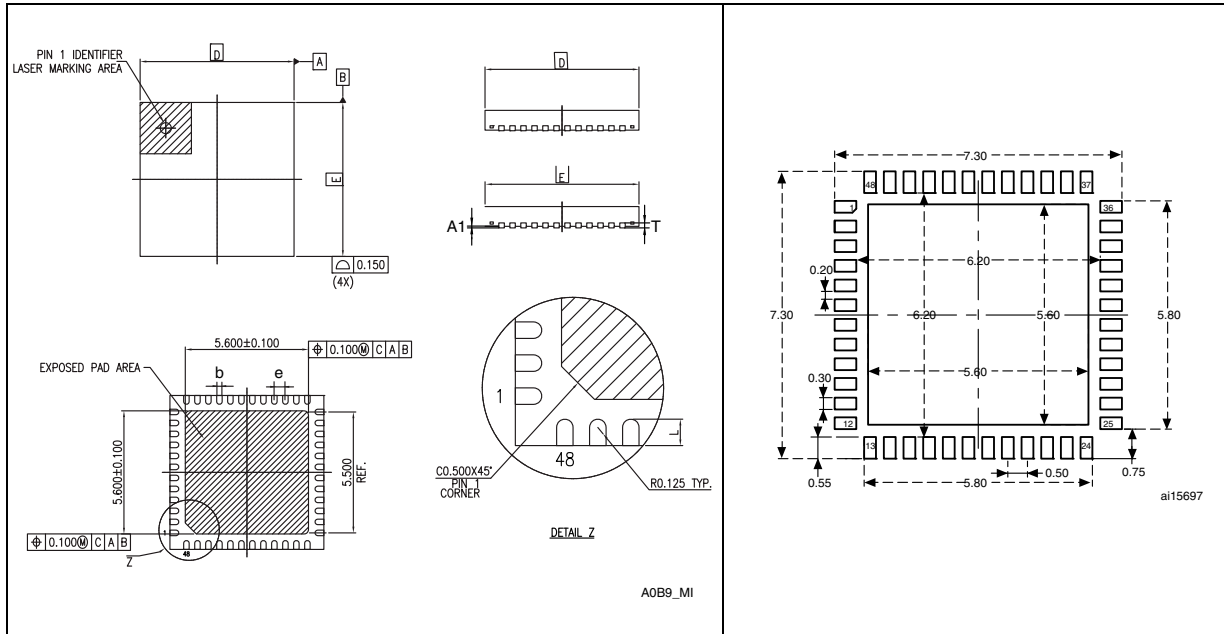
1. Drawing is not to scale.

2. All leads/pads should also be soldered to the PCB to improve the lead/pad solder joint life.

3. There is an exposed die pad on the underside of the UFQFPN package. It is recommended to connect and solder this back-side pad to PCB ground.

Table 12. UFQFPN48 7 x 7 mm, 0.5 mm pitch, package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A	0.500	0.550	0.600	0.0197	0.0217	0.0236
A1	0.000	0.020	0.050	0.0000	0.0008	0.0020
D	6.900	7.000	7.100	0.2717	0.2756	0.2795
E	6.900	7.000	7.100	0.2717	0.2756	0.2795
L	0.300	0.400	0.500	0.0118	0.0157	0.0197
T		0.152			0.0060	
b	0.200	0.250	0.300	0.0079	0.0098	0.0118
e		0.500			0.0197	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Marking of engineering samples

Figure 14. UFQFPN48 package top view
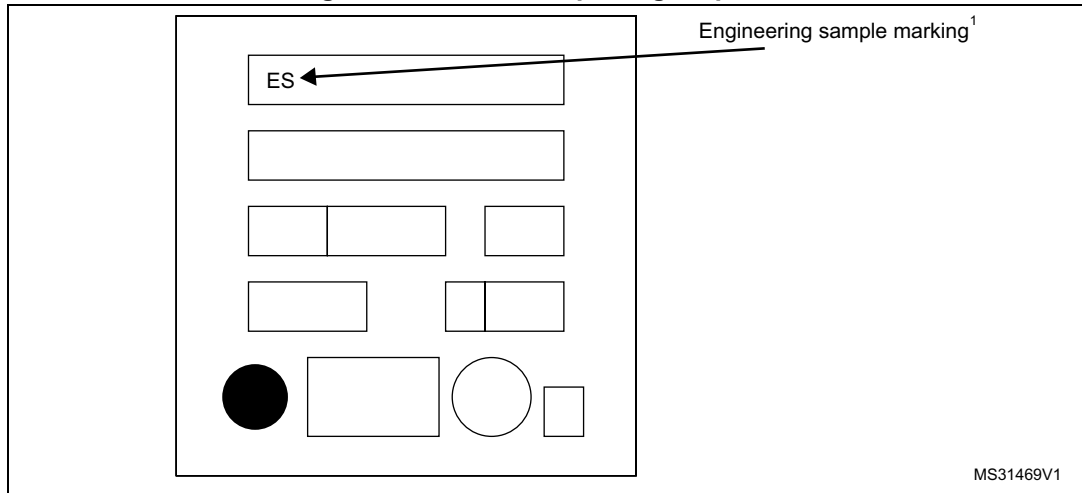
Engineering sample marking[1]

ES

MS31469V1

1. Devices identified with "ES" are engineering samples intended to be sent to the customer for electrical compatibility evaluation. They may be used to start customer qualification. Therefore, ST is not liable for any customer usage in production and/or in reliability qualification trials.

5.1.3   LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package

Figure 15. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package outline[1]
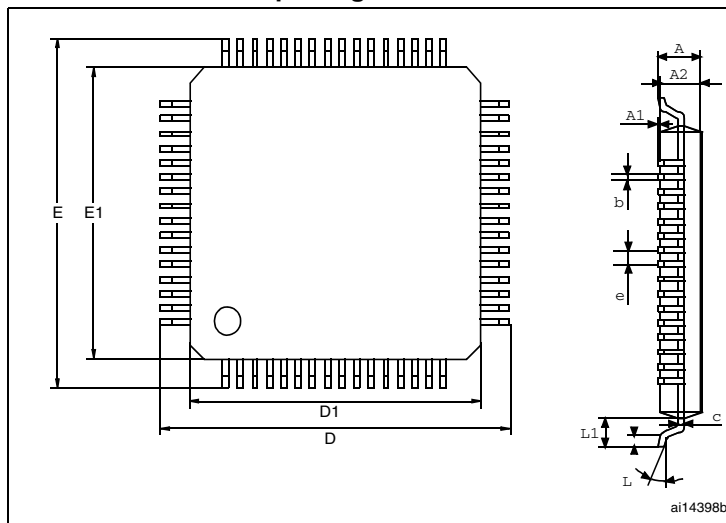
Figure 16. Recommended footprint[1][2]

ai14398b

ai14909
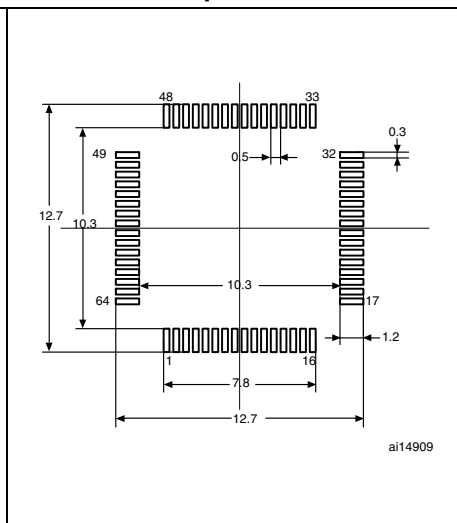
1. Drawing is not to scale.

2. Dimensions are in millimeters.

Table 13. LQFP64, 10 x 10 mm, 64-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.60			0.0630
A1	0.05		0.15	0.0020		0.0059
A2	1.35	1.40	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.20	0.0035		0.0079
D		12.00			0.4724	
D1		10.00			0.3937	
E		12.00			0.4724	
E1		10.00			0.3937	
e		0.50			0.0197	
θ	0°	3.5°	7°	0°	3.5°	7°
L	0.45	0.60	0.75	0.0177	0.0236	0.0295
L1		1.00			0.0394	
N	**Number of pins**					
	64					

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Marking of engineering samples

Figure 17. LQFP64 top view
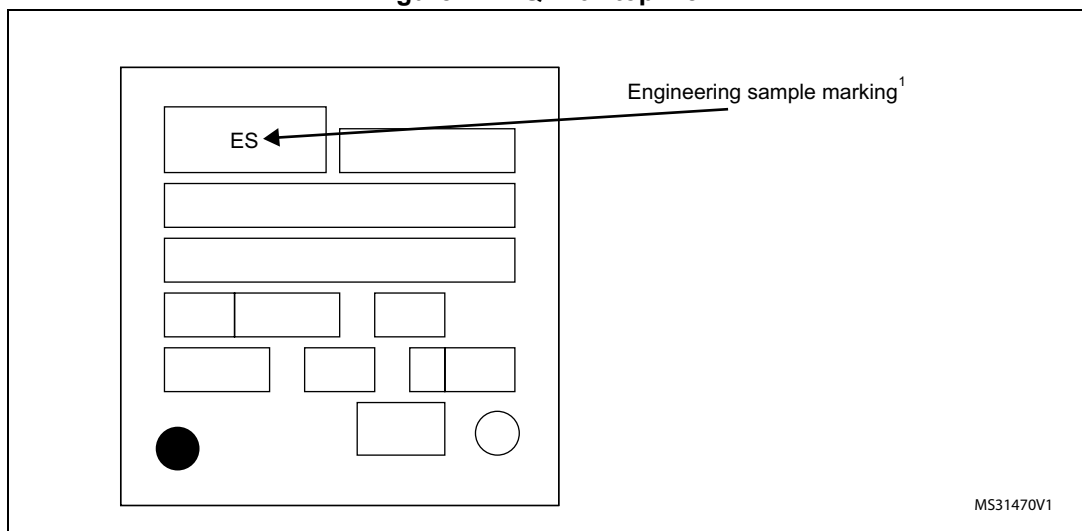
1. Devices identified with "ES" are engineering samples intended to be sent to the customer for electrical compatibility evaluation. They may be used to start customer qualification. Therefore, ST is not liable for any customer usage in production and/or in reliability qualification trials.

Figure 18. LQFP100, 14 x 14 mm, 100-pin low-profile quad flat package outline[1]

Figure 19. Recommended footprint[1][2]
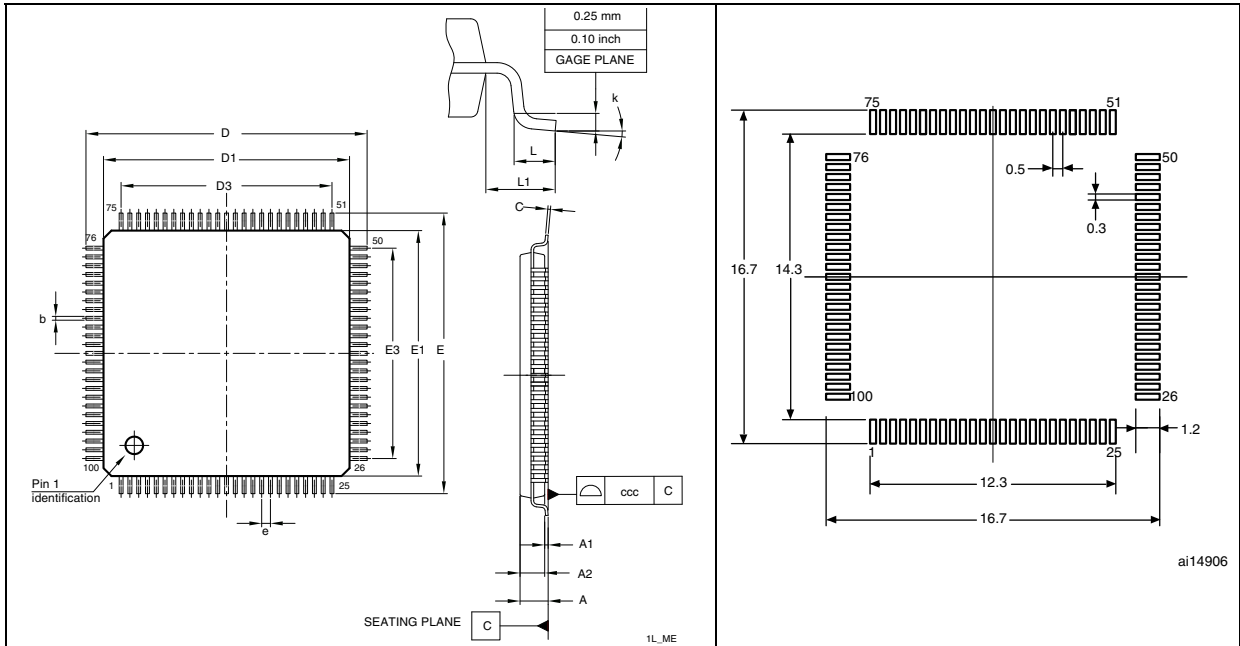
1. Drawing is not to scale.

2. Dimensions are in millimeters.

Table 14. LQPF100, 14 x 14 mm, 100-pin low-profile quad flat package mechanical data

Symbol	millimeters			inches[1]		
	Min	Typ	Max	Min	Typ	Max
A			1.6			0.063
A1	0.05		0.15	0.002		0.0059
A2	1.35	1.4	1.45	0.0531	0.0551	0.0571
b	0.17	0.22	0.27	0.0067	0.0087	0.0106
c	0.09		0.2	0.0035		0.0079
D	15.8	16	16.2	0.622	0.6299	0.6378
D1	13.8	14	14.2	0.5433	0.5512	0.5591
D3		12			0.4724	
E	15.8	16	16.2	0.622	0.6299	0.6378
E1	13.8	14	14.2	0.5433	0.5512	0.5591
E3		12			0.4724	
e		0.5			0.0197	
L	0.45	0.6	0.75	0.0177	0.0236	0.0295
L1		1			0.0394	
k	0.0°	3.5°	7.0°	0.0°	3.5°	7.0°
ccc		0.08			0.0031	

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Marking of engineering samples

Figure 20. LQPF100 top view
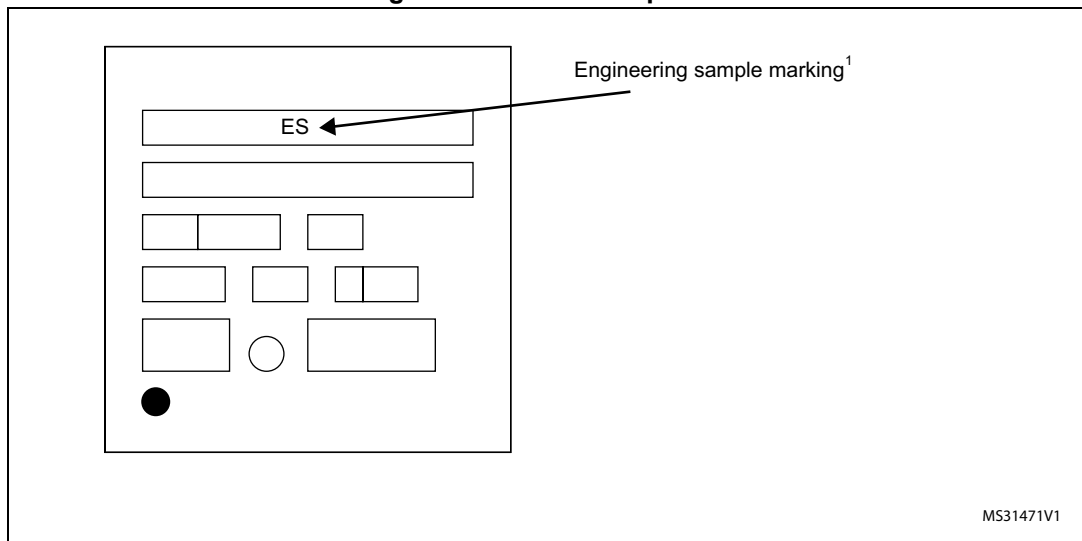
1. Devices identified with "ES" are engineering samples intended to be sent to the customer for electrical compatibility evaluation. They may be used to start customer qualification. Therefore, ST is not liable for any customer usage in production and/or in reliability qualification trials.

6 Ordering information scheme

Table 15. Ordering information scheme

Example: STM32 F401C C T 6 xxx

Device family
STM32 = ARM-based 32-bit microcontroller

Product type
F = General-purpose

Device subfamily
401: 401 famly

Pin count
C = 48/49 pins
R = 64 pins
V = 100 pins

Flash memory size
B = 128 Kbytes of Flash memory
C = 256 Kbytes of Flash memory

Package
T = LQFP
U = UFQFPN
Y = WLCSP

Temperature range
6 = Industrial temperature range, –40 to 85 °C

Packing
TR = tape and reel
No character = tray or tube

7   Revision history

Table 16. Document revision history

Date	Revision	Changes
26-Apr-2013	1	Initial release.

Please Read Carefully: