Macroblock

LED Driver ICs- General Application Note

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April 03, 2007

We Light Up Your LEDs

Foreword

- PrecisionDrive™ series provide outstanding performance. However, there are still conditions to use the driver correctly.
- This application note provides basic criteria for LED module designs. So, “general” is called.
- Following the guidelines, chip users (module designers) are able to generate not only feasible (workable) designs but also cost-effective (reliable) engineering solutions.

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1. DC Operating Points

- 1.1 DC operating point
- 1.2 Minimum of V_{DS}
- 1.3 Maximum of V_{DS} under the limitation of heat dissipation
- 1.4 Maximum Power Dissipation
- 1.5 Cascade LEDs vs. Max. Power Dissipation
- 1.6 Solution to Minimizing Total VF Deviation
- 1.7 Example for a lighting solution (MBI1816)
- 1.8 Rext and Rtrim

1.1 DC Operating Point

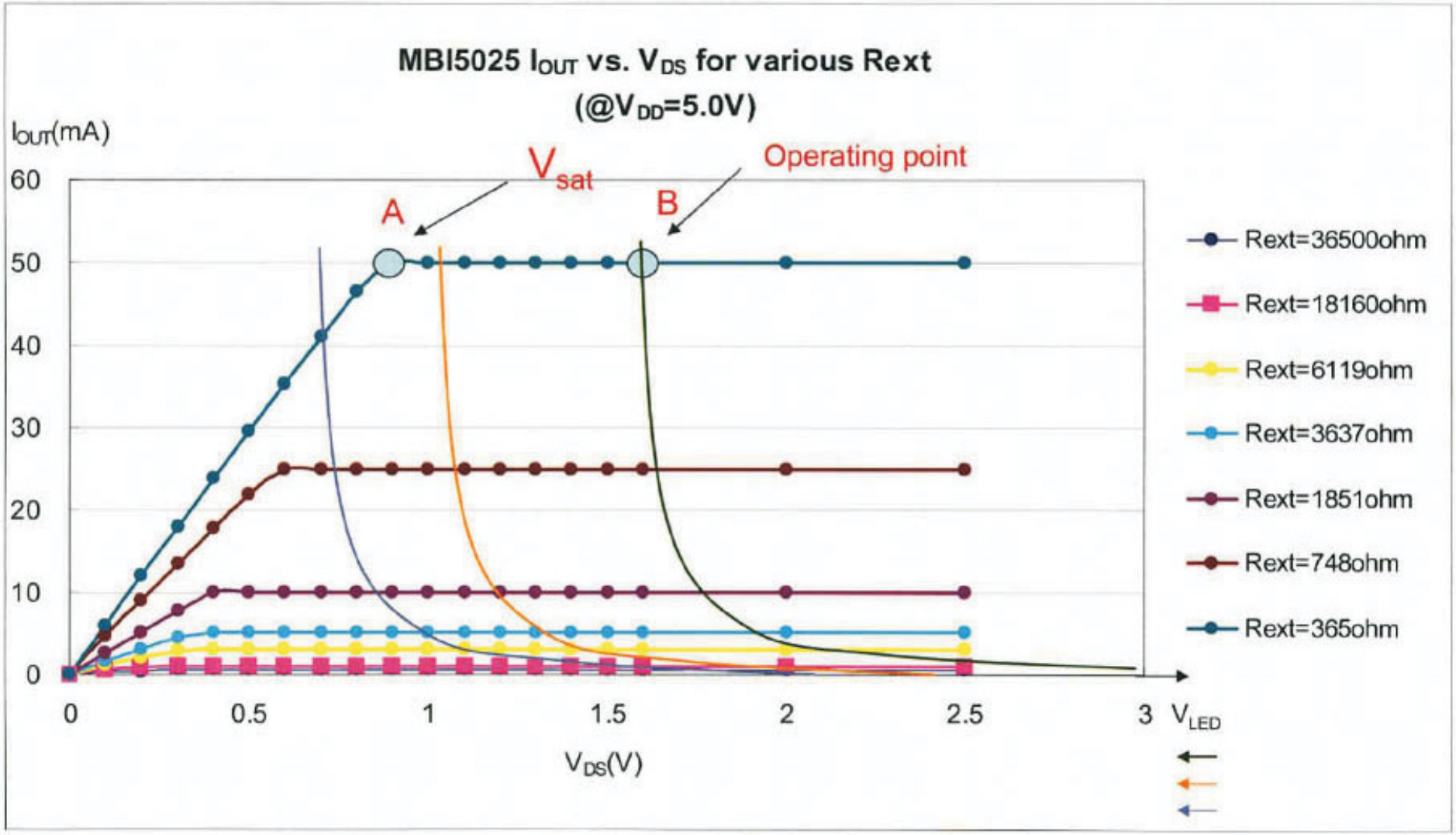


Fig. 1.

1.2 Minimum of V_{DS}

- Considerations of operating point, minimum of V_{DS}
  - Both V_{LED} and V_F determine V_{DS}
    - If V_{LED} is too high, causing V_{DS} being too high, this will lead to heating problem in driver ICs.
  - $V_{DS} > V_{sat}$, where V_{sat} is saturation point (i.e 0.7V@50mA)
    - In order to keep constant current
  - $V_{DS} = V_{LED} - V_{F,max} - V_{DROP} > V_{sat}$, where V_F is LED forward voltage, and $V_{F,min} \leq V_F \leq V_{F,max}$ in LED's datasheet.

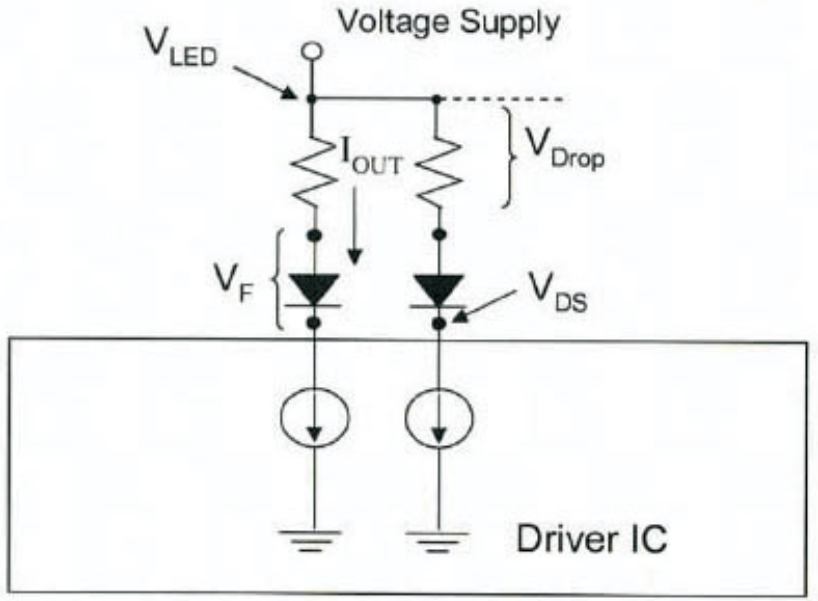


Fig. 2.

1.3 Maximum of V_{DS} under the limitation of heat dissipation

- Maximum of V_{DS} is limited by power dissipation
  - $P_{D(act)} = V_{DD} \times I_{DD} + V_{DS} \times I_{OUT} \times N$, where N is LED channel numbers.

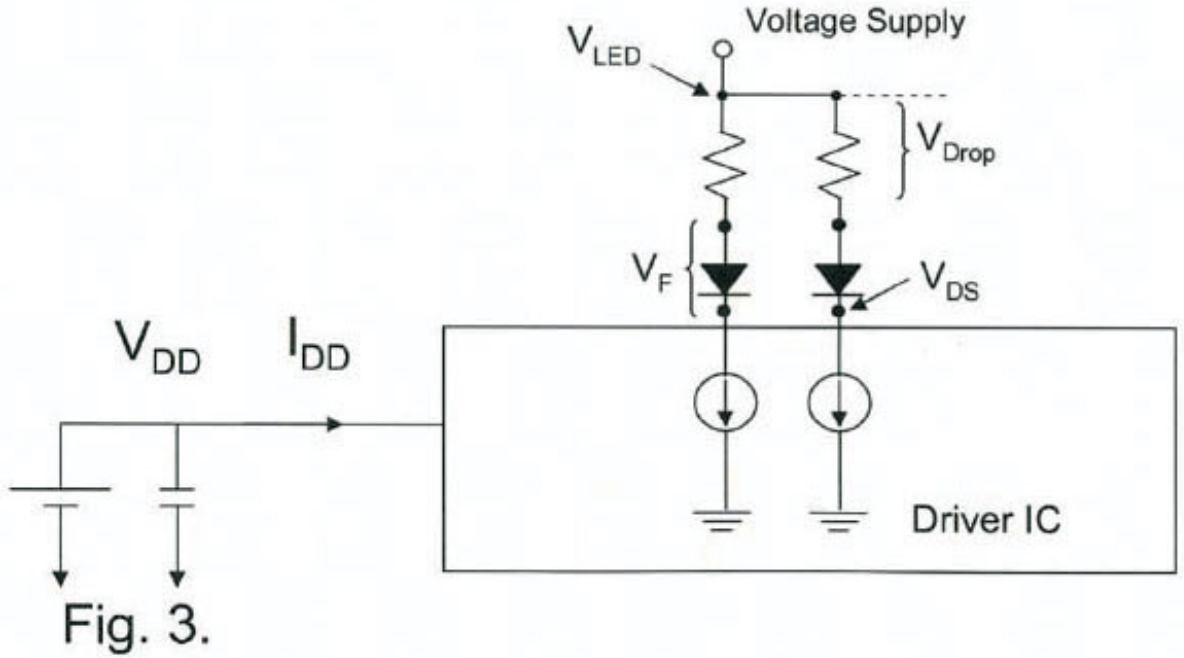


Fig. 3.

Lower voltage of V_{DS} can obtain lower power dissipation. Therefore, DC operating point slightly larger and approaching the saturation point is better.

1.4 Maximum Power Dissipation

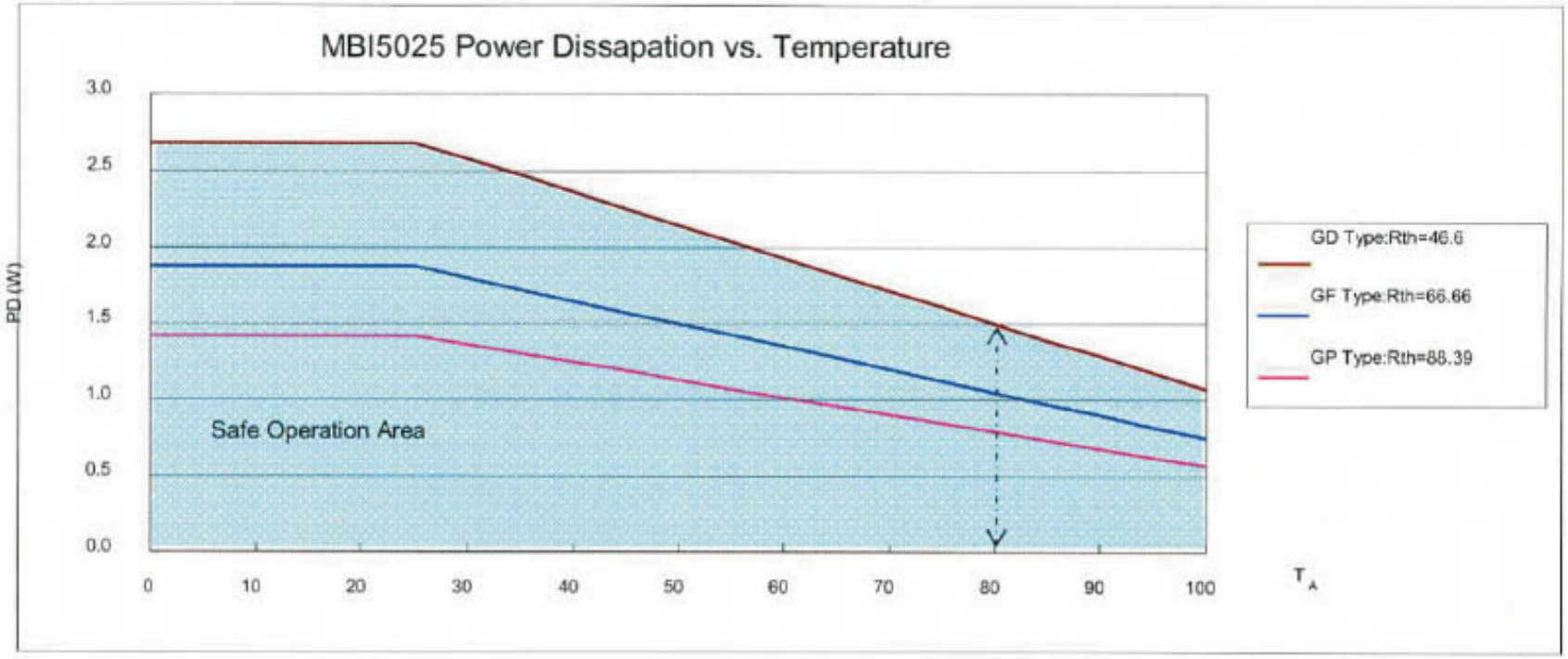


Fig. 4.

When the driver ICs are operated at more than 80°C,

P_D should be <1.5W for GD type to keep ICs in the safe operation area.

P_D should be <1.0W for GF type to keep ICs in the safe operation area.

P_D should be <0.8W for CP type to keep ICs in the safe operation area.

1.5 Cascade LEDs vs. Max. Power Dissipation

The yellow color is needed to be fill in by customer			
MBI1816 Calculation	**RED LED for Lighting**		
Conditions	1	2	
V_{LED} (Applied Voltage)	17	17	V
	VF-max	VF-min	
V_F (LED)	2	1.8	V
LED Current / per string	0.04	0.04	A
LED Series numbers / per string	8	8	pcs
IC's Output pin voltage(Vds) @ 40mA/Channel Suggest 0.7V at least@ 40mA / per channel	0.70	2.30	V
Series resistor between V_{LED} and LED	7.50	7.50	Ohm
Pd on series resistor	0.01	0.01	Watt
Total IC's Pd@40mA / per channel	0.448	1.472	Watt

The tolerance of V_F will probably lead to driver IC over heating

1.6 Solution to Minimizing Total VF Deviation

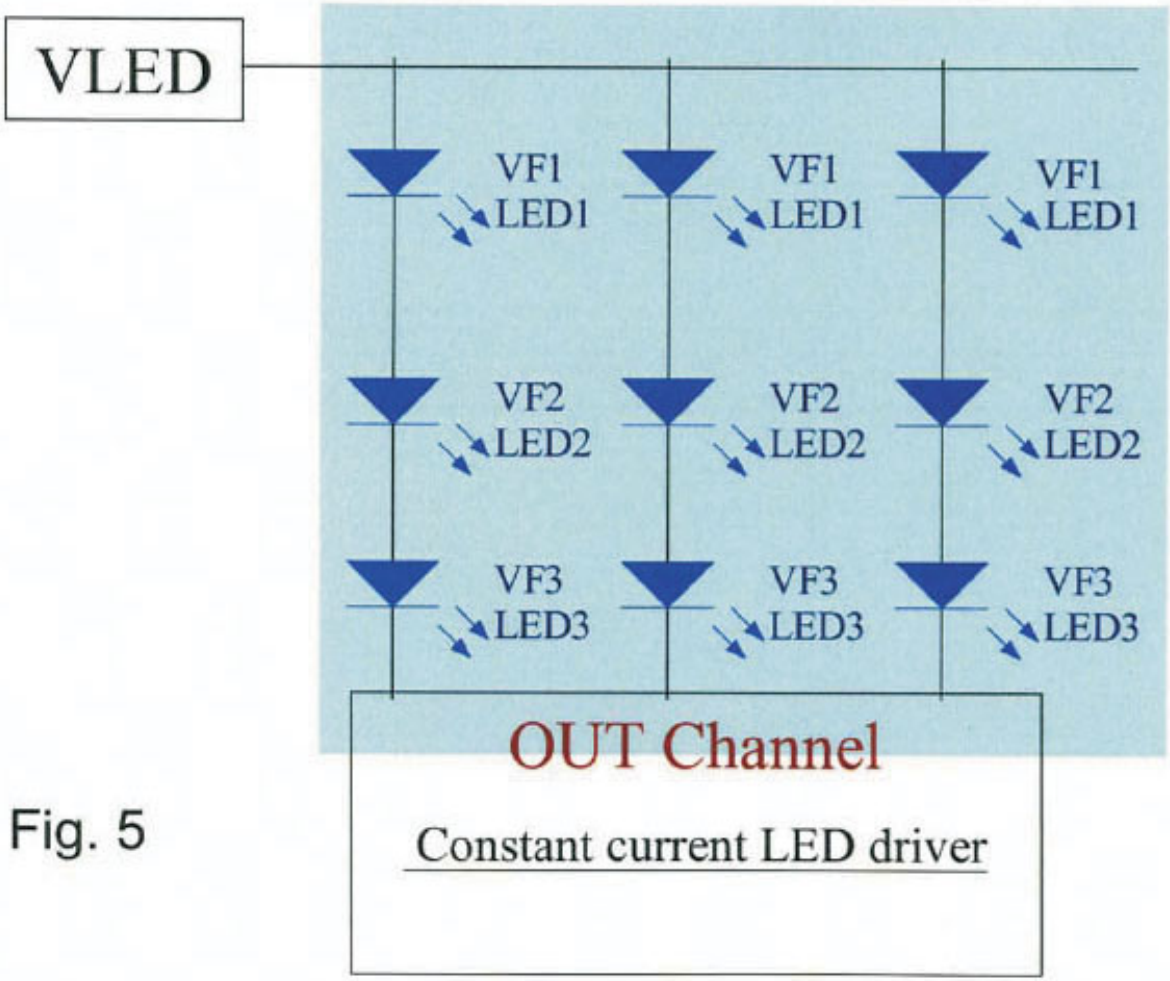


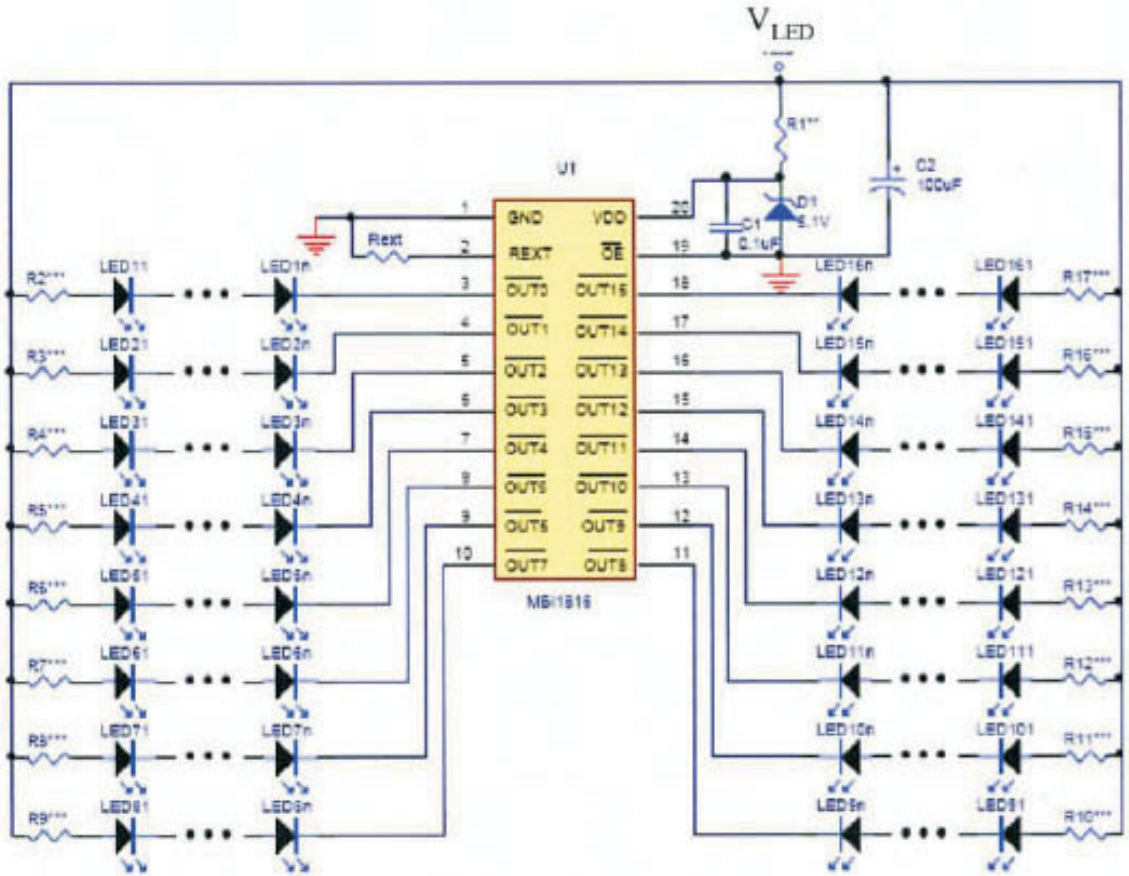
Fig. 5

If VF1,VF2,VF3 are sorted by bins

}:Total VF= VF1+VF2+VF3

The power dissipation of each output channel will be very close.

1.7 Example for a Lighting Solution (MBI1816)



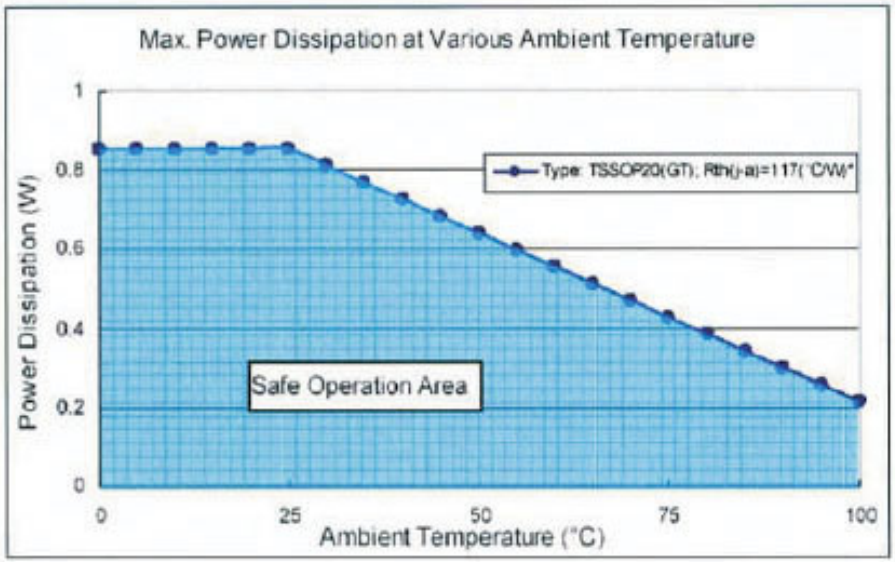


Fig. 6

* $V_{LED} > V_{DS} + V_{F,LED} \times n$; $V_{F,LED}$: Forward voltage of LED; n: LED count
** R1 = (V_{LED} - 5.1V) / I_{DD}; refer to Electrical Characteristics for I_{DD}
*** R2~R17 = [$V_{LED} - V_{DS} - (V_{F,LED} \times n)$] / I_{LED}

1.8 Rext and Rtrim

Setting Output Current in a Group

- R_{trim} and R_{ext}
  - $R_{ext}=R_o+ N \times R_{trim}$, where N is IC number.

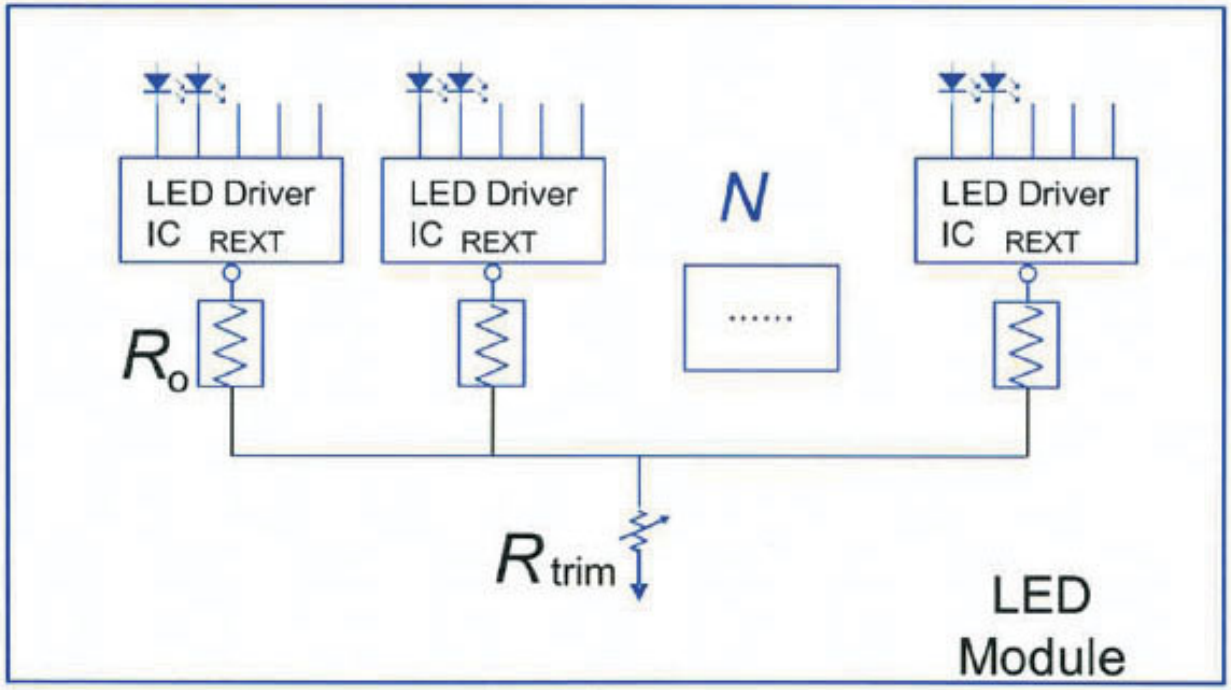


Fig. 7

Constraint: $N*R_{trim}<R_o/3$; otherwise, the chip skew will be not good.

2. Digital Signals

- 2.1 Digital Signals
- 2.2 Minimum Pulse Width of /OE
- 2.3 Signal Conditioning
- 2.4 Delay Matching
- 2.5 Logic Level
- 2.6 Buffer output capacity

2.1 Digital Signals

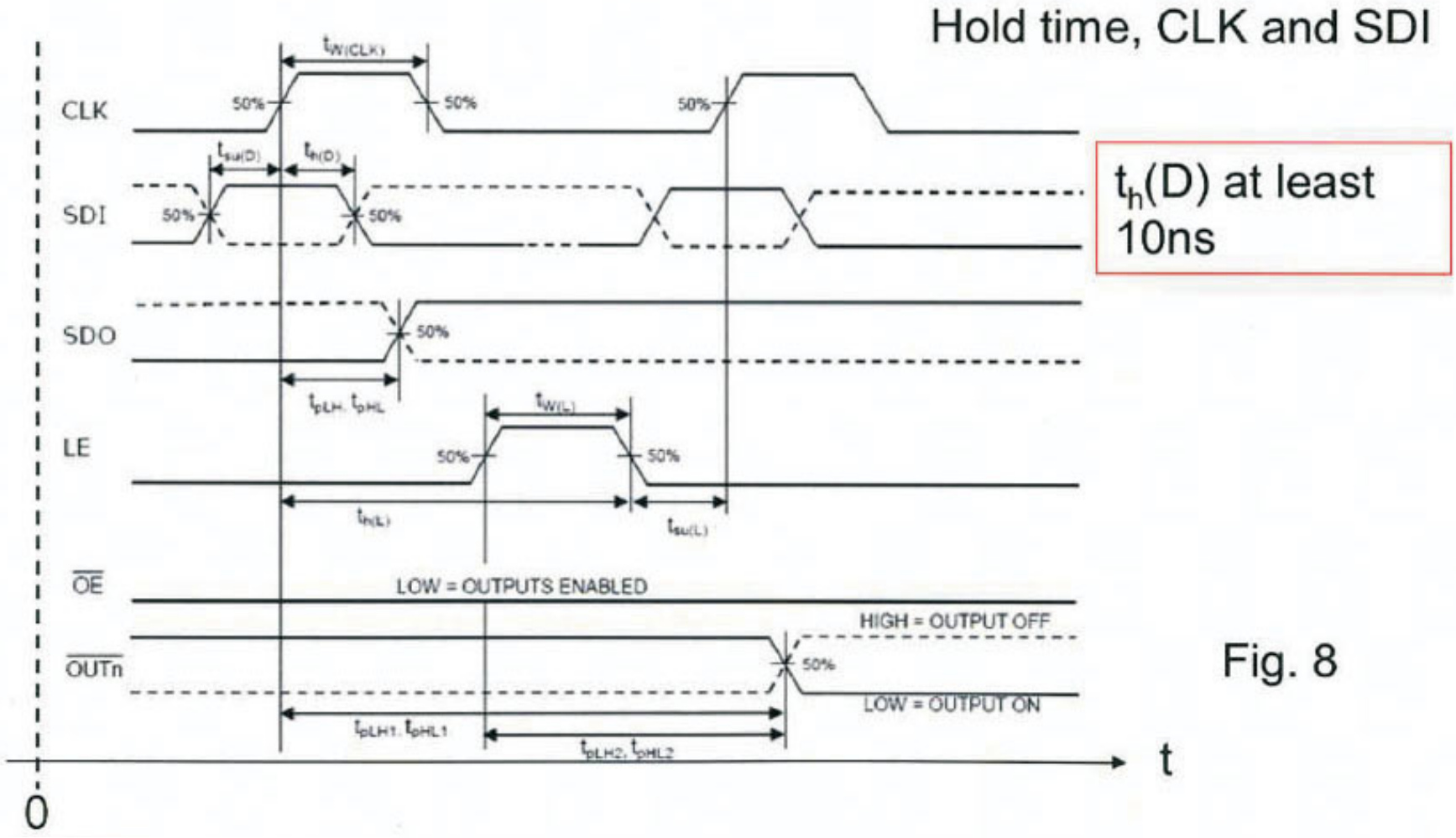


Fig. 8

2.2 Minimum Pulse Width of /OE

- The relationship between /OE and /OUT

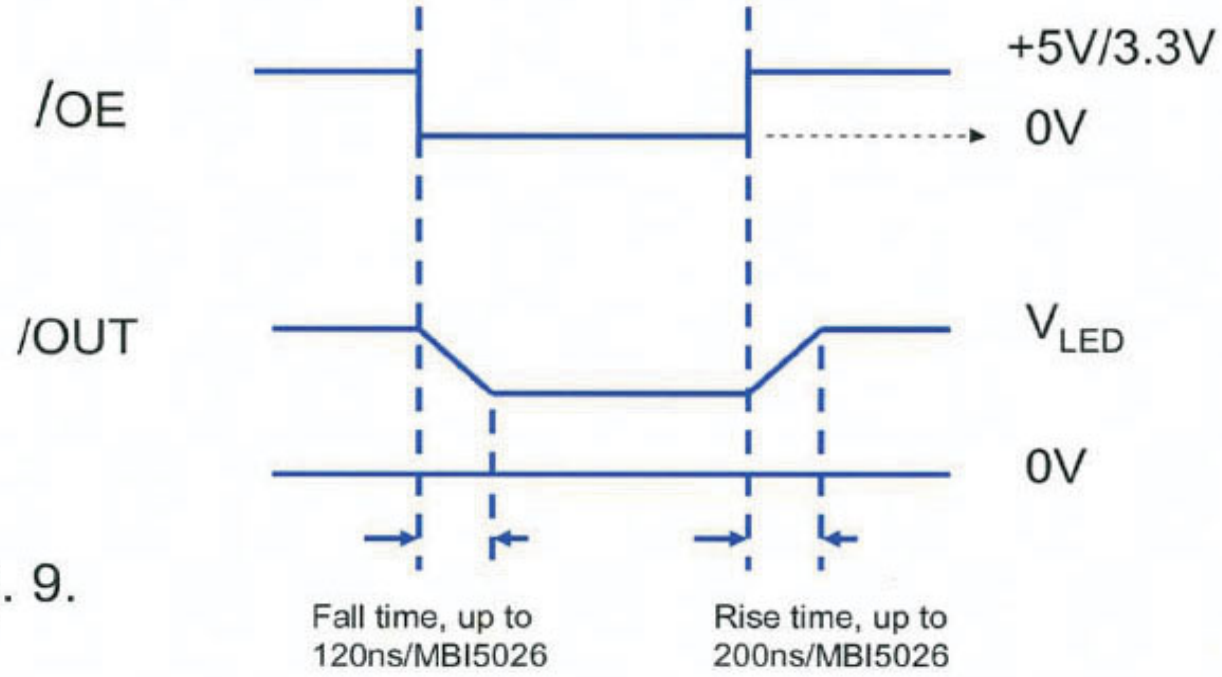


Fig. 9.

If /OE pulse width is less than 320 ns, the effective output pulse width will be distorted. Additional compensation to PWM will be necessary.

2.3 Signal Conditioning

Check digital signals, CLK, LE, and /OE

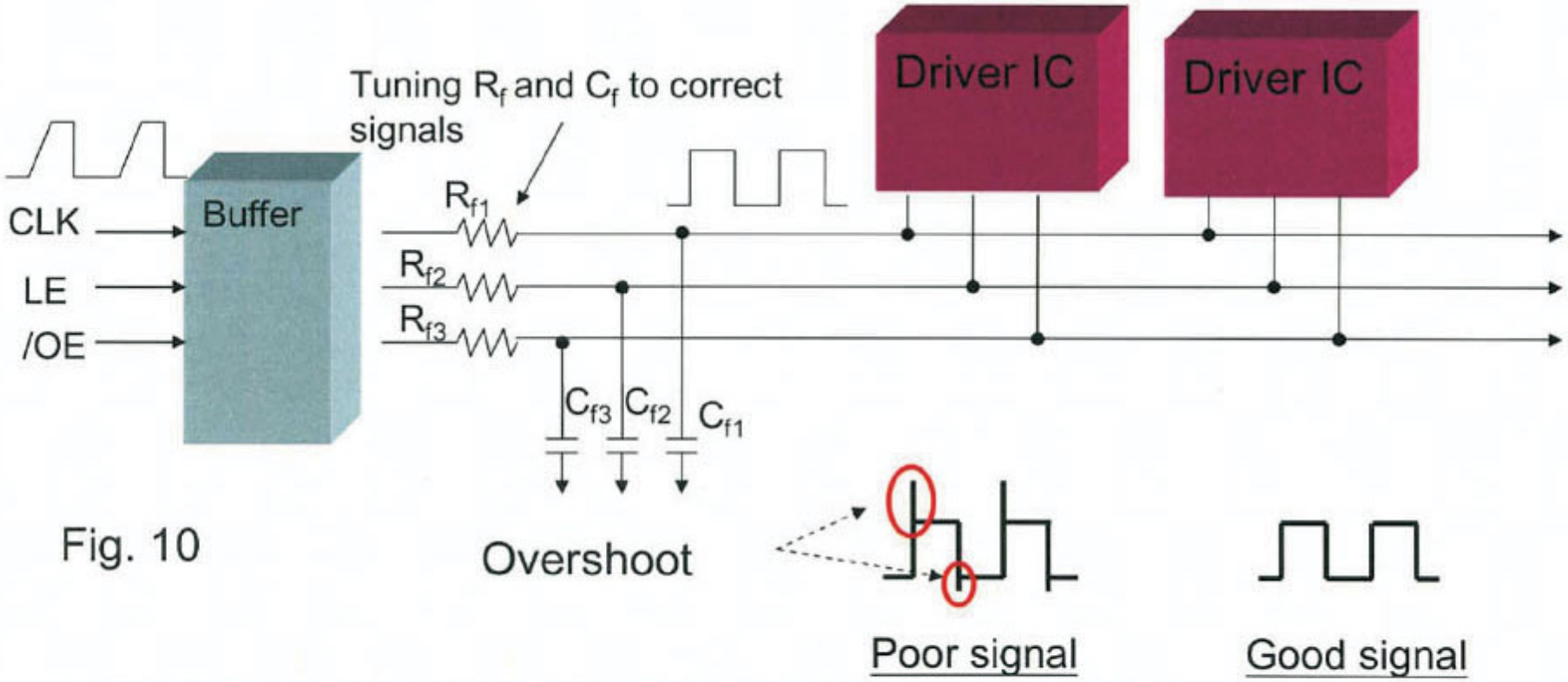


Fig. 10

If the input port of driver IC receives the over driving signals, it will be probably damaged by the signals, which will then increase the IC temperature.

2.4 Delay Matching

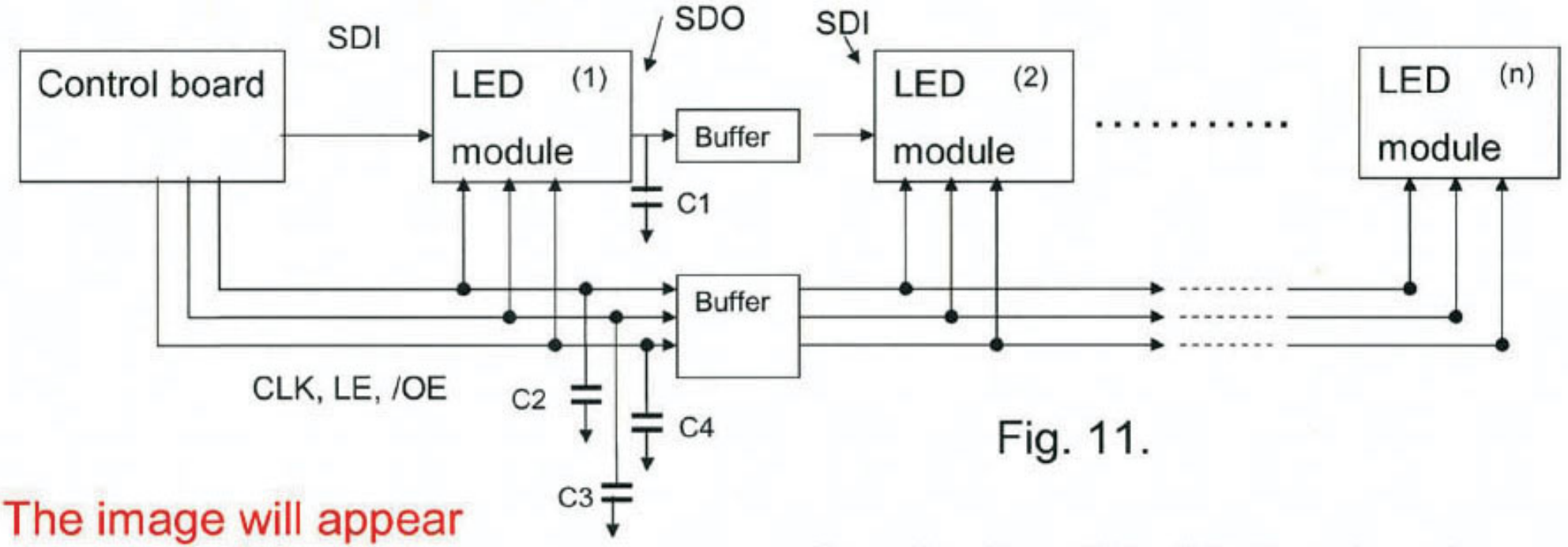


Fig. 11.

The image will appear abnormal, if the logic signal does not occur in the right timing. SDI vs. CLK is especially critical.

By adjusting C1~C4, the signals of SDI, CLK, LE and /OE may follow the exact timing shown as Fig. 6.

2.5 Logic Level

- The necessary voltage levels to transmit valid logic 1 and logic 0 are: $V_{IH} > 0.8xV_{DD}$, and $V_{IL} < 0.3xV_{DD}$
  - When V_{DD} =5V, V_{IH} = 4.0V and V_{IL} < 1.5V
- 74HCxxx buffer will be required, rather than 74LSxxx buffer.

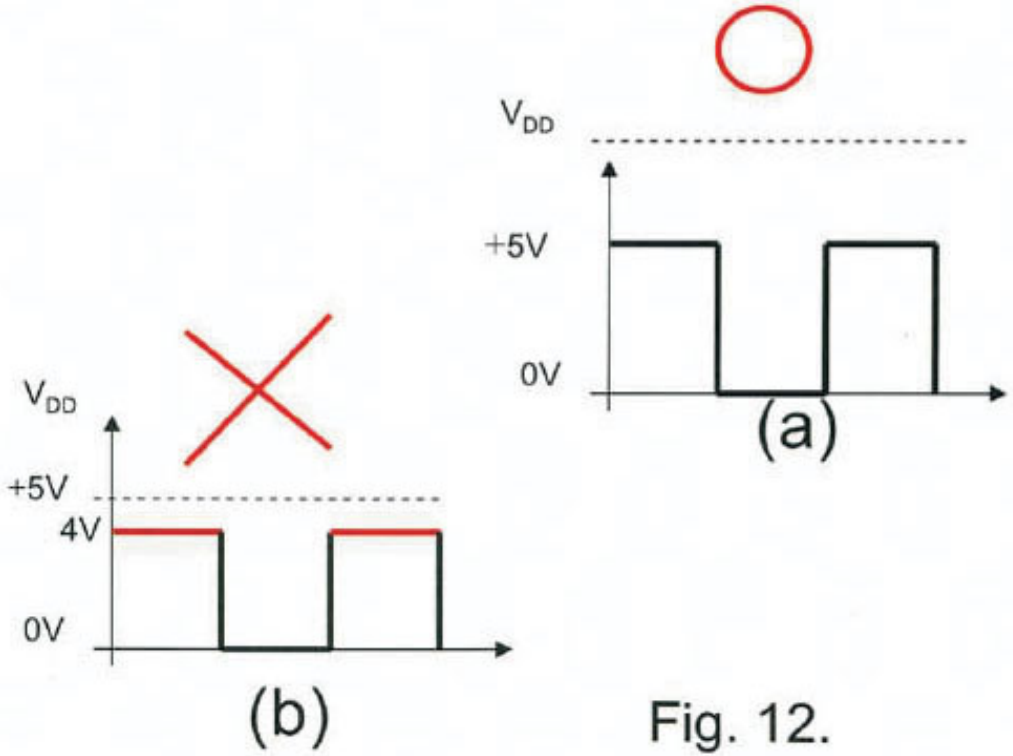
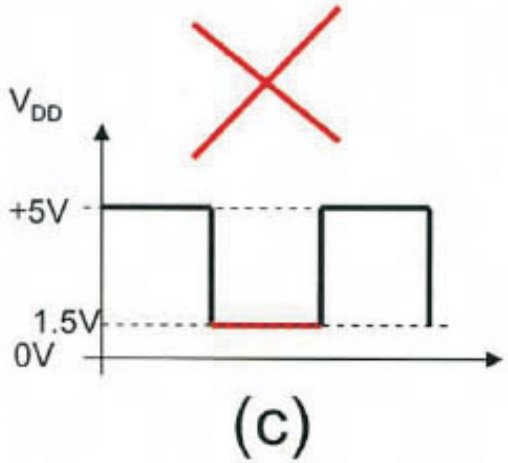


Fig. 12.

The image will appear abnormal, if the logic level does not transmit in the right voltage range.



2.6 Buffer Output Capacity

- In general, the LED display board will need signal buffer to driver LED driver. Further, one signal buffer will driver several LED drivers in a LED display board. A reference equation to calculate the number of LED drivers connecting to buffer's output port, it is shown as following. Assume that Vdd is 5V for buffer.
  - $N_1=I_{source,buffer}/(Vdd/250K)$, $N_2=I_{sink,buffer}/(Vdd/250K)$, The two numbers, N_1 and N_2, the smaller one is the number of LED drivers connecting to buffer's output port.
  - Where $I_{source,buffer}$ is the minimum source current shown in buffer's datasheet, and $I_{sink,buffer}$ is the minimum sink current shown in buffer's datasheet.

3. Switching Noise and Circuit Layout

- 3.1 Switching noise on V_{DD}
- 3.2 Solution 1
- 3.3 Solution 2
- 3.4 Solution 3
- 3.5 Overshoot
- 3.6 Voltage Spike Damages Driver IC
- 3.7 Placement of Drivers on PCB
- 3.8 Placement of Drivers off PCB
- 3.9 Placement of Capacitors
- 3.10 Solving voltage drop with paralleling wires connector
- 3.11 Oscillation at OUT pins
- 3.12 Vrext oscillation
- 3.13 Power Supply's EMI Suppression

3.1 Switching Noise on V_{DD}

- When V_{DD} is disturbed by a high-frequency noise, the driver IC might malfunction
  - If V_{DD} and V_{LED} are connected to the same supply voltage source, as shown in Fig. 11(b), V_{DD} will be very noisy.
  - The temperature on the driver IC will increase and cause the damage of driver IC.

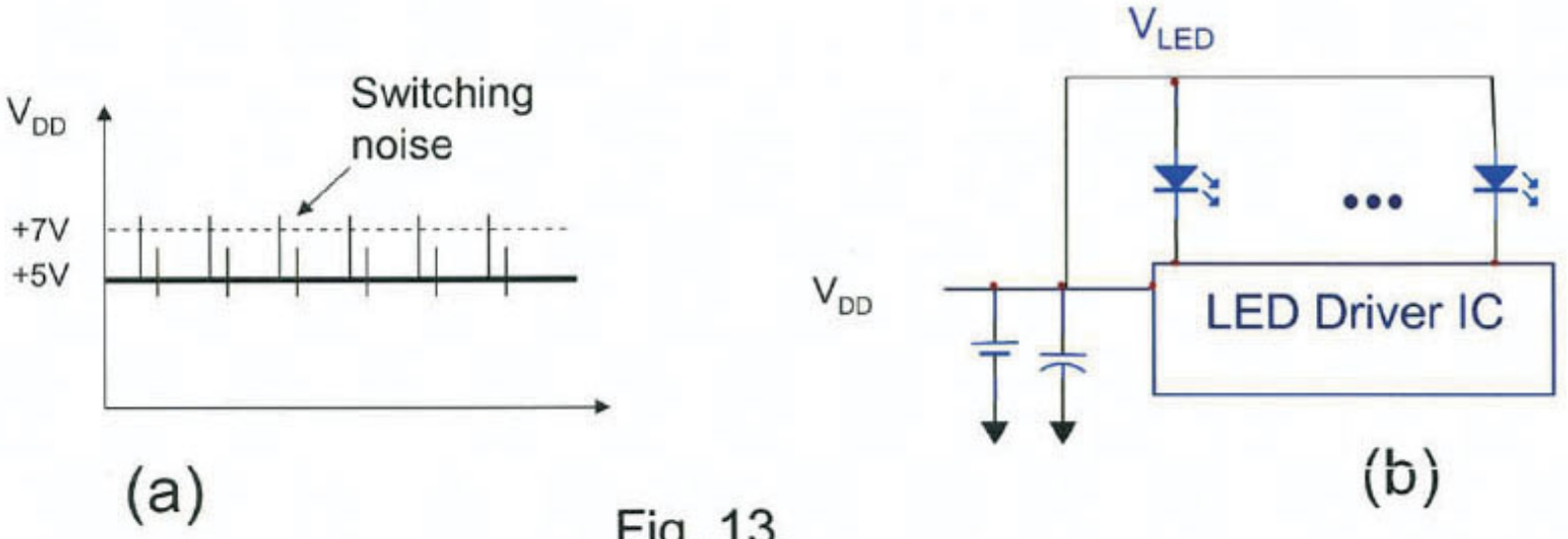


Fig. 13.

3.2 Solution 1

- To separate V_{DD} from V_{LED},
  - Even though they are the same voltage level

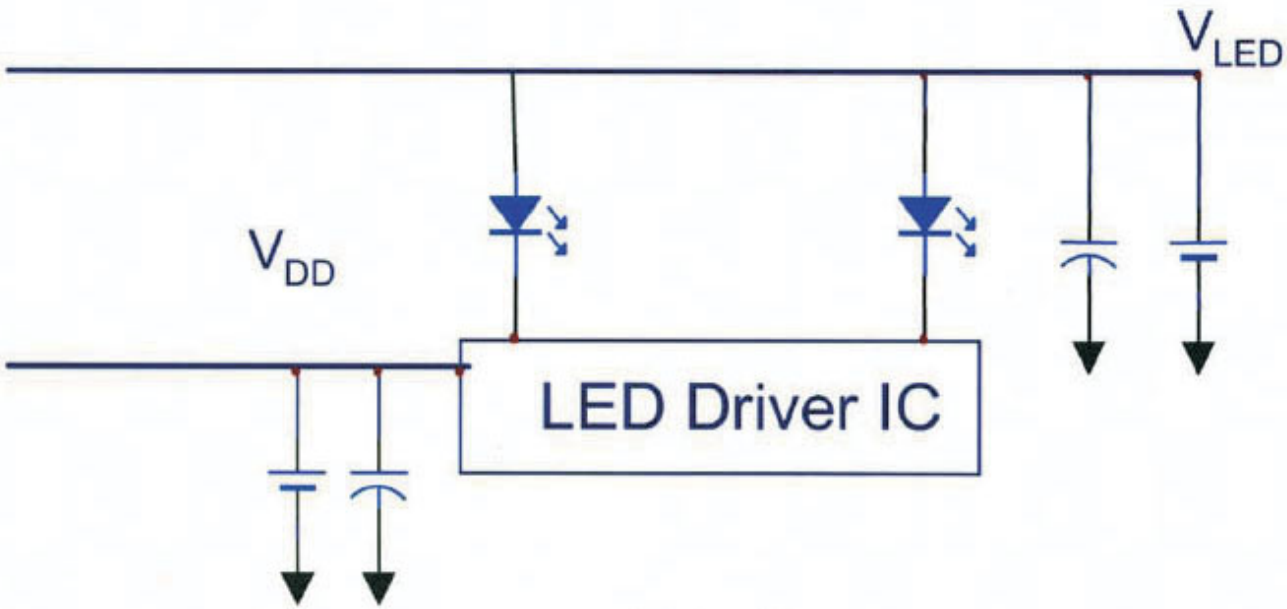


Fig. 14.

3.3 Solution 2

- To add an inductor in series between V_{DD} and V_{LED}, in case there is only one voltage source
- To add two capacitors for V_{DD} and V_{LED} individually

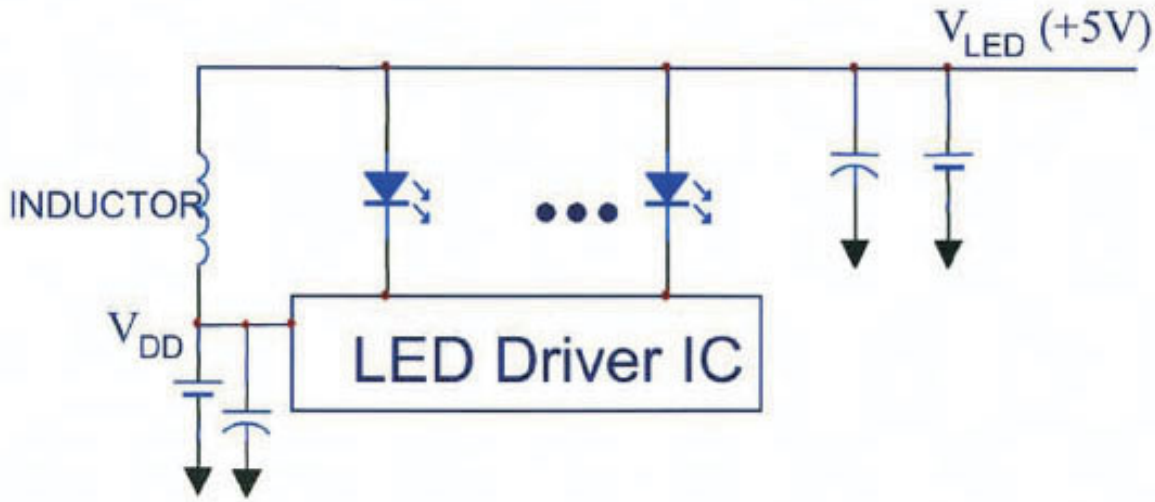


Fig. 15.

3.4 Solution 3

- To add a capacitor (C1) beside the transistor in parallel in time-multiplexing application (dynamic/ scan type)

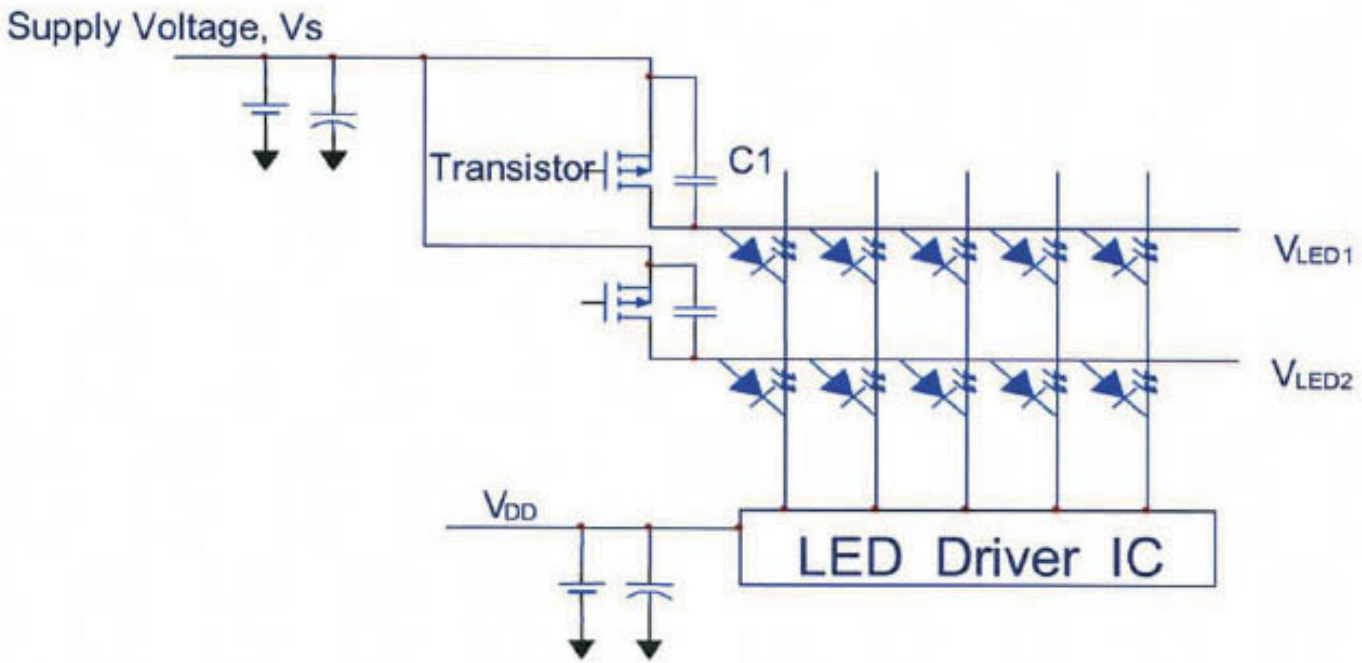


Fig. 16-a.

- To add a capacitor (C_2) across Gate and Gnd or to add resistor R_1 in series with Gate terminal in order to reduce the switching speed of MOSFET.

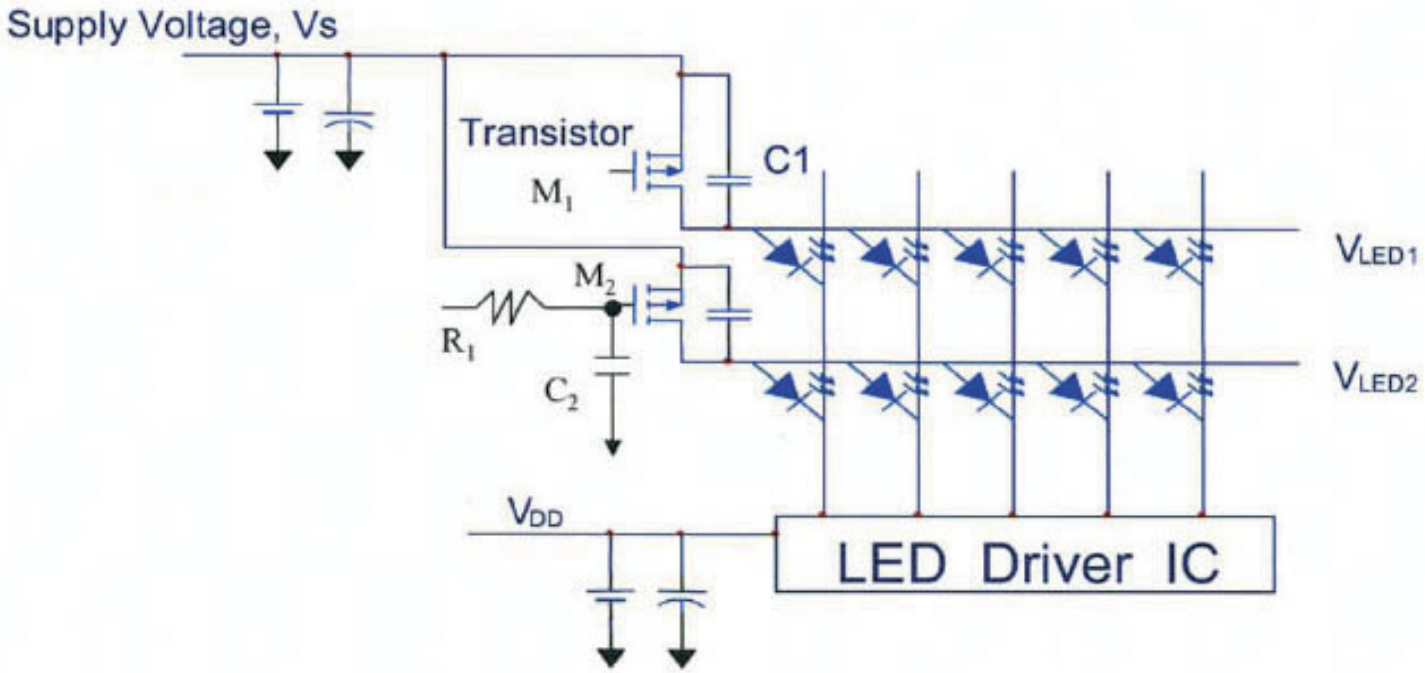


Fig. 16-b

- If the switching noise was caused by fast rising time of driver IC, provide the release loop for magnetic energy in parasitic inductor by adding Schottky diodes from the $V_{LED1,2}$ To V_{LED}.

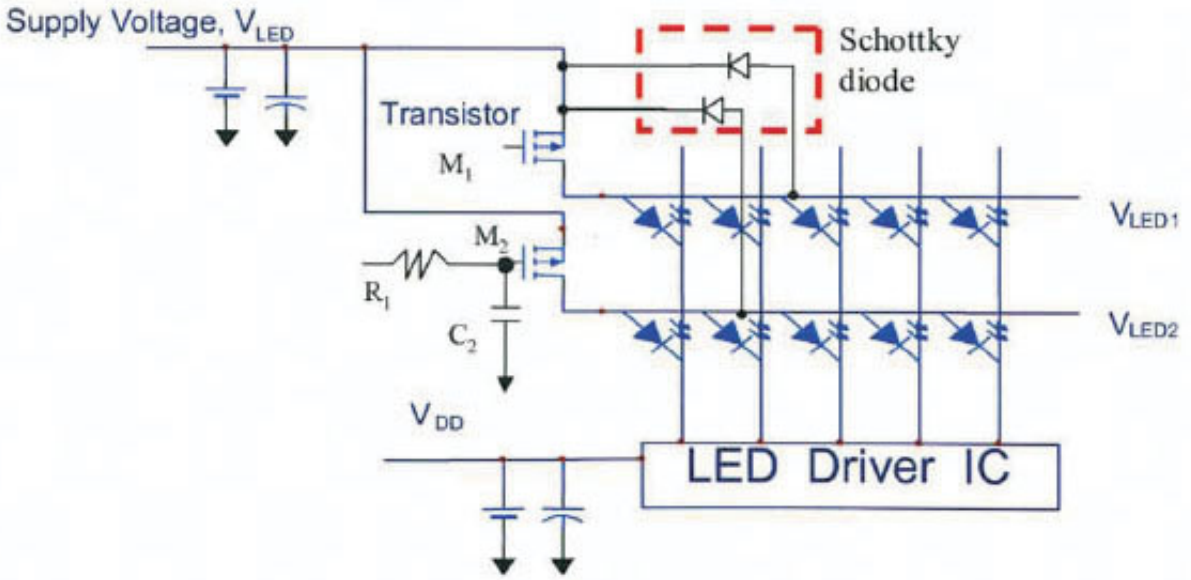


Fig. 16-c

3.5 Overshoot

- What is voltage overshoot at OUT pin?

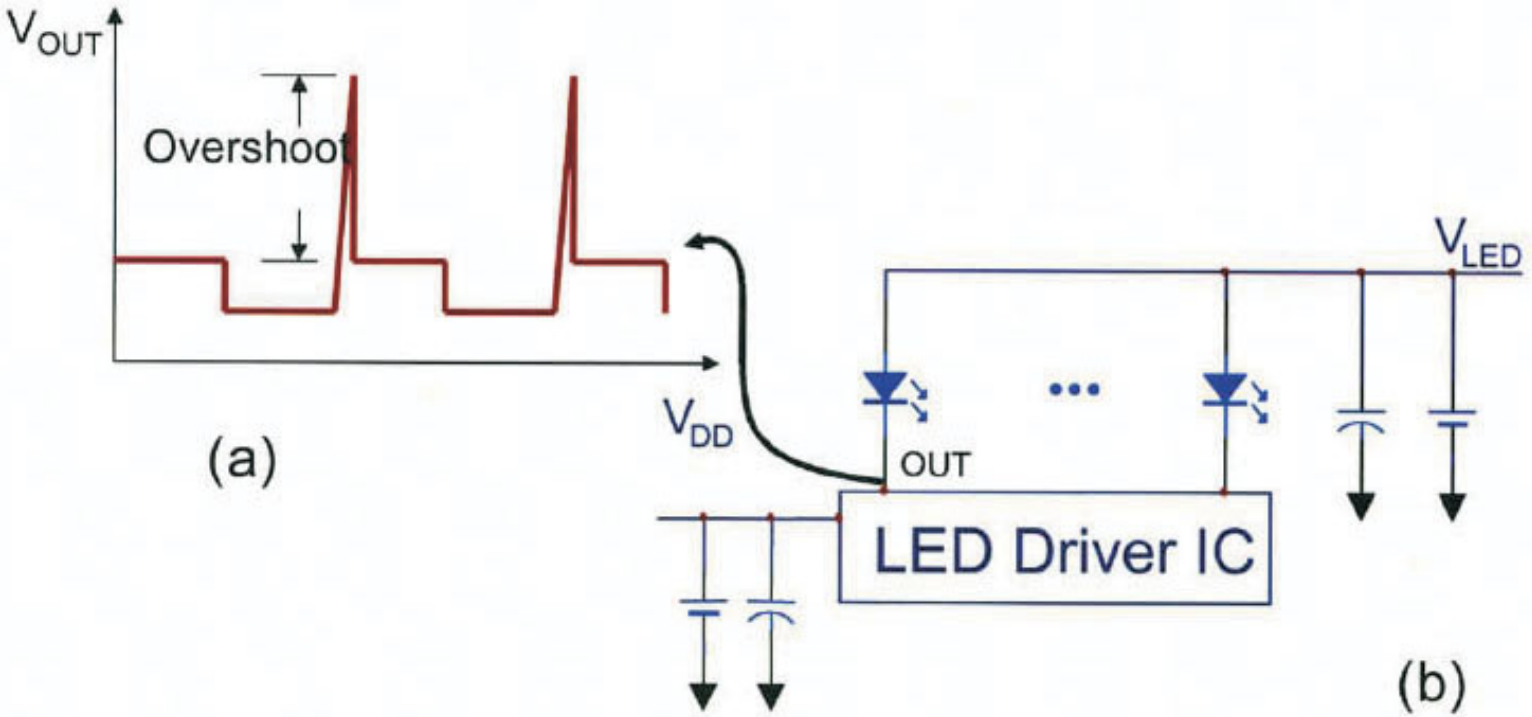


Fig. 17.

How does the overshoot come?

$$V_L = L \times \frac{dI_{LED}}{dt_{rise}}$$

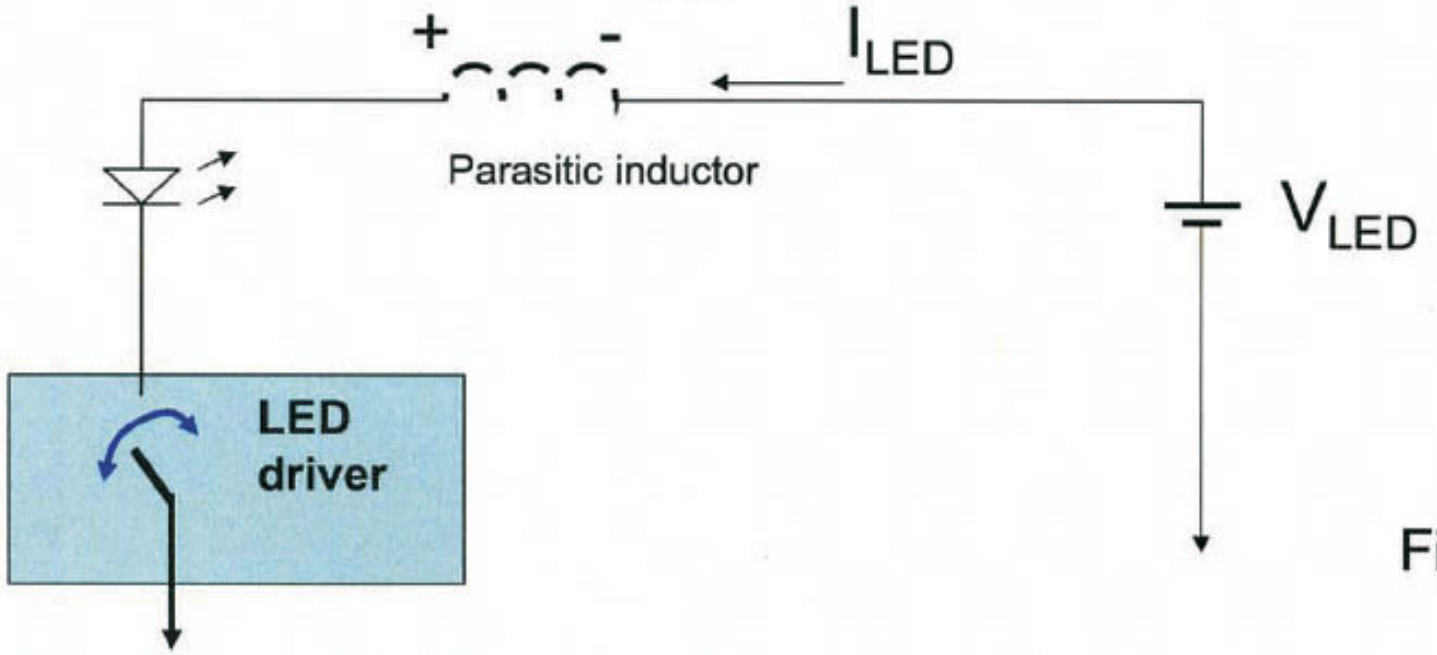


Fig. 18.

A significant parasitic inductor will result in high voltage spike in /OUT pins. Shorter conduction line will have smaller parasitic inductor.

- The overshoot will probably damage IC's /OUT pins if the voltage spike has enough energy.
- In addition, if V_{DD} is not separated from V_{LED}, V_{DD} may be affected by the voltage spike.

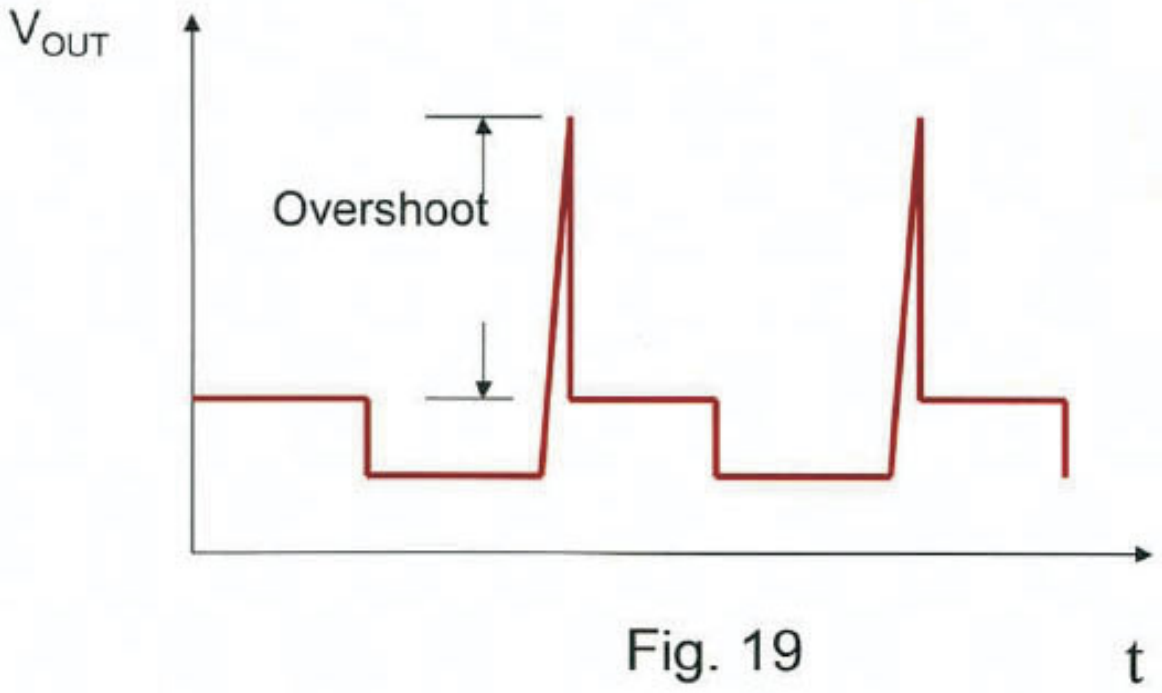


Fig. 19

3.6 Voltage Spike Damages Driver IC

- Two conditions of voltage spike that damages driver IC.
  - Condition 1: The peak of the voltage spike is over 17V.

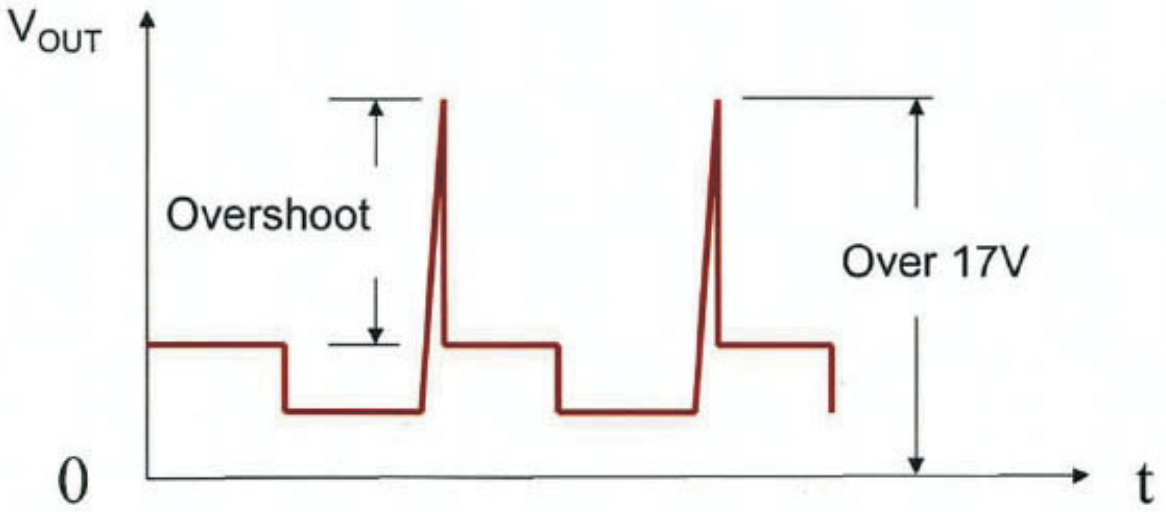


Fig. 20

- Condition 2: When the voltage spike is under 17V while ½ pulse width of the voltage spike is smaller than the delay time between /OE and /OUT, the voltage spike will damage the driver IC.
  - For example, per MBI5026 datasheet, the voltage spike of output pin is 7V and the ½ pulse width is smaller than 150ns.

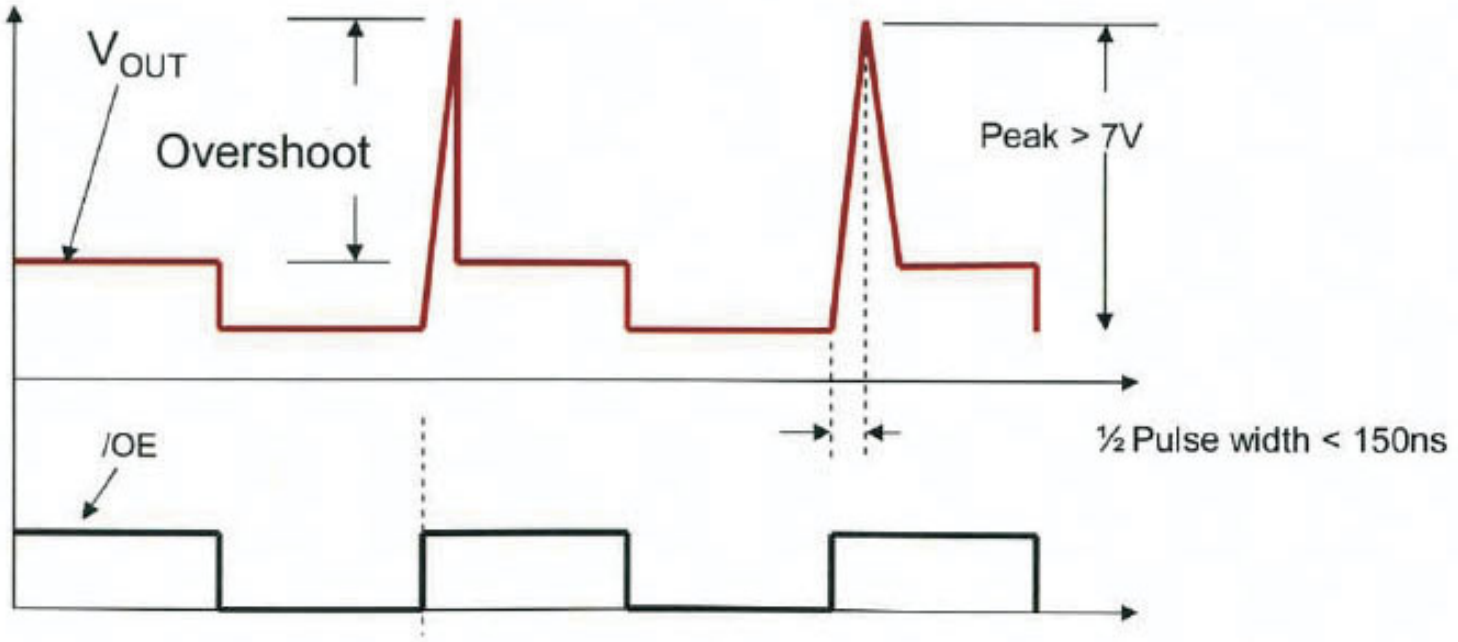


Fig. 21.

3.7 Placement of Drivers on PCB

- The Driver IC should be geographically as close to the LED as possible.

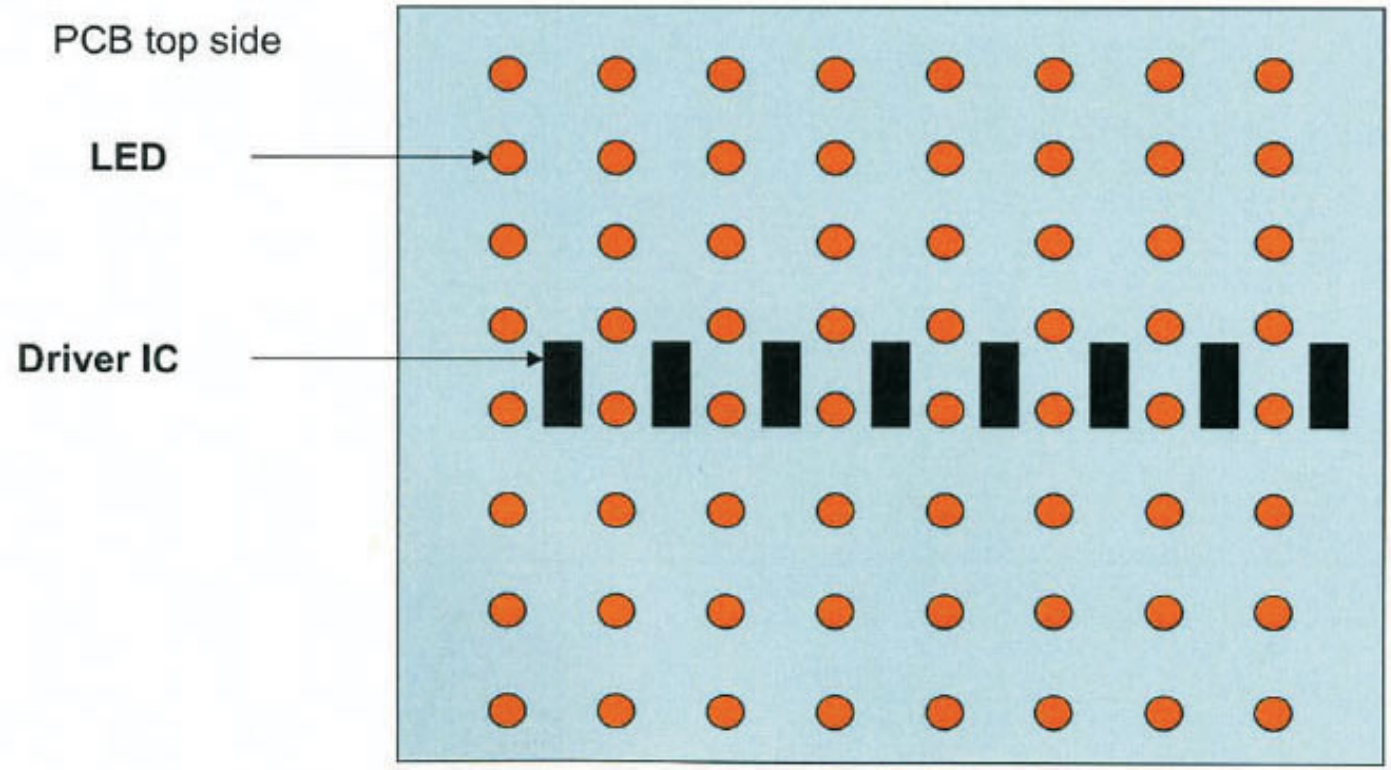
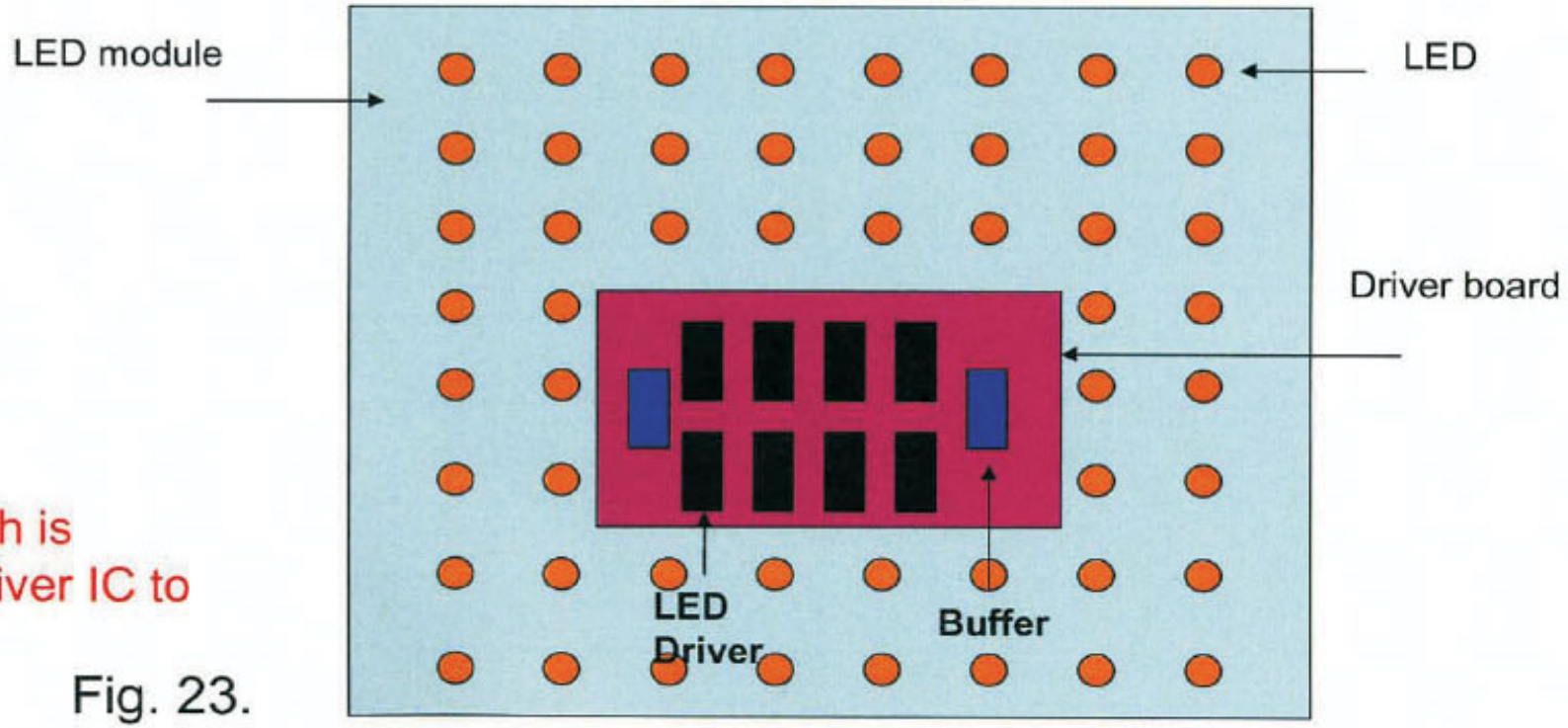


Fig. 22.

3.8 Placement of Drivers off PCB

- In some cases, the driver ICs are placed on another driver board and the driver board is connected to an LED module.
- For LED modules with wide pitches, 30 mm, the wire is long, from driver IC to LED.



The wire length is longer from driver IC to LED.

Fig. 23.

3.9 Placement of Capacitors

- Distributed capacitors for V_{LED}

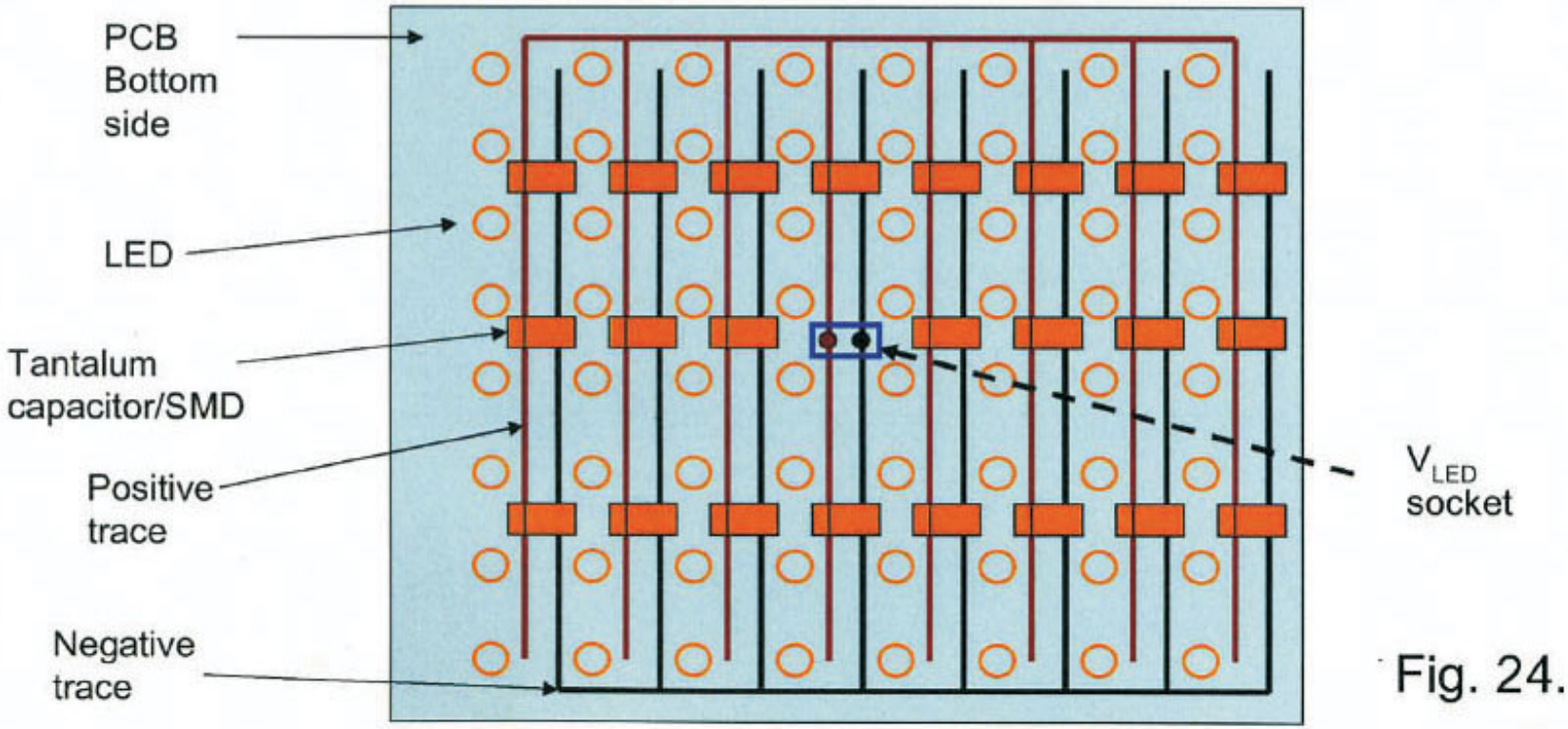


Fig. 24.

Placement of Capacitors

- Poor arrangement regarding capacitors for V_{LED}

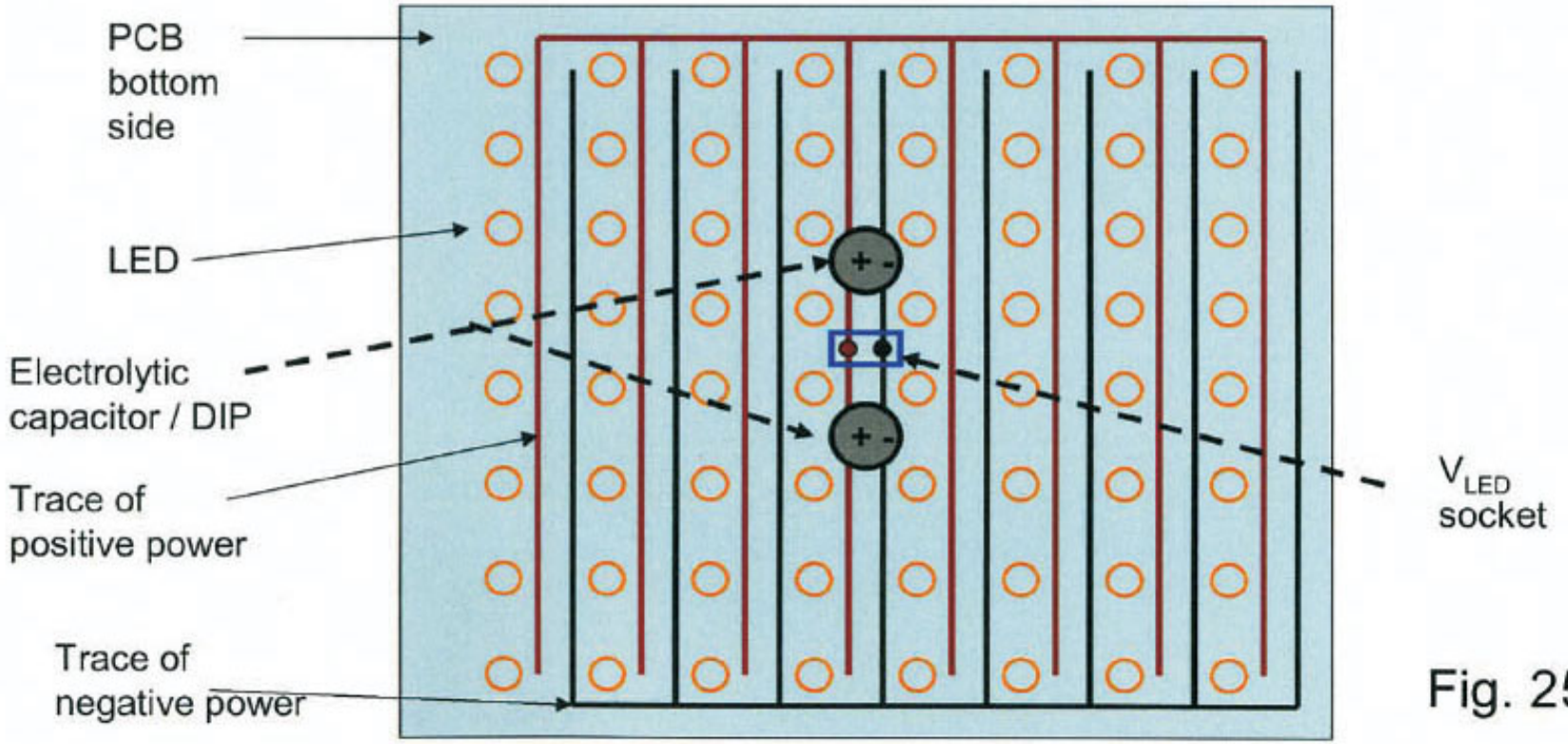


Fig. 25.

3.10 Reducing The Voltage Drop in The Long Conduction Line

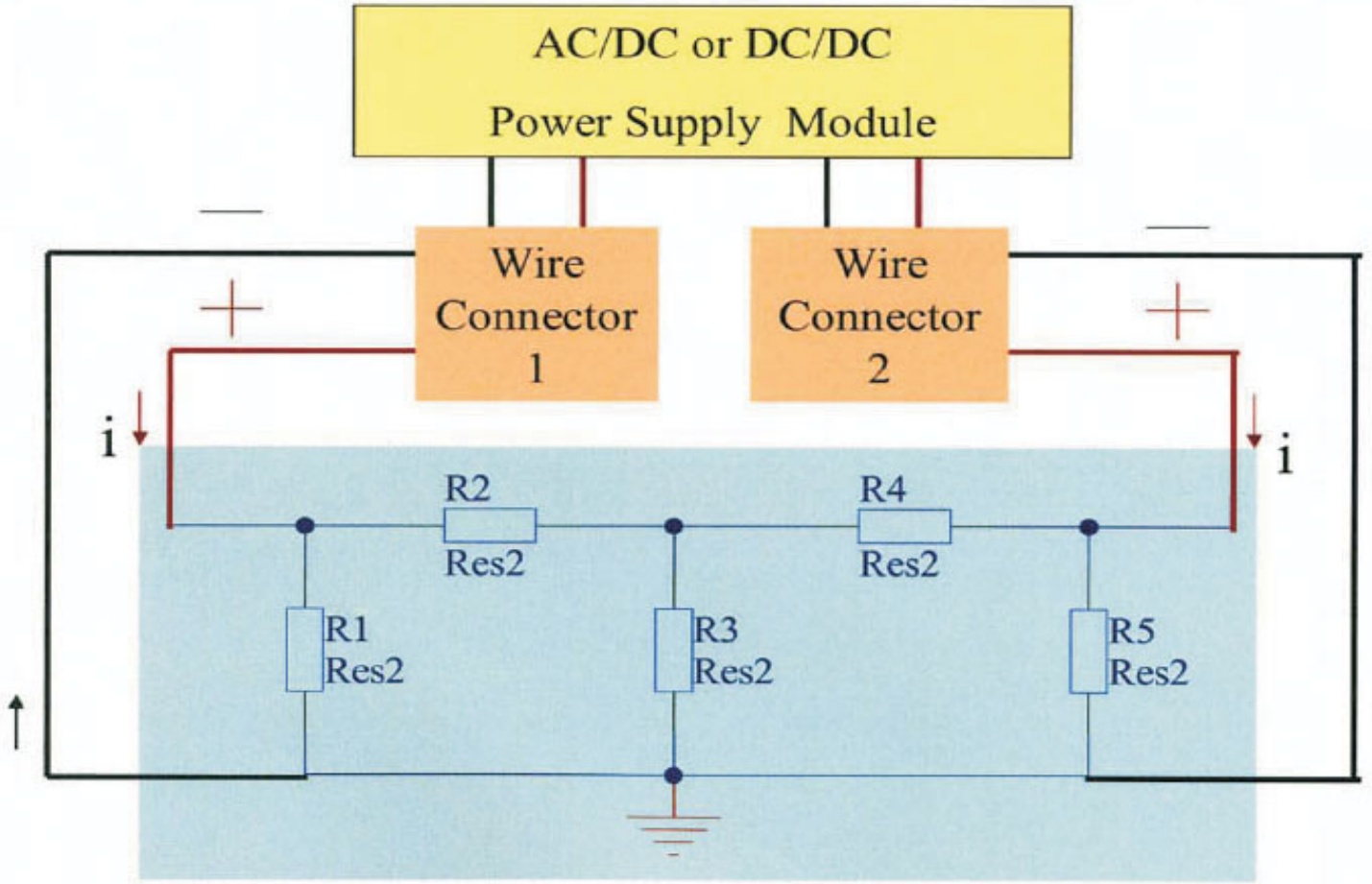


Fig. 26

If a voltage source are not on PCB's center, provide power source on two terminals to reduce voltage drop on long conduction line.

3.11 Oscillation at OUT pins

- The oscillation occurs usually with a poor phase margin inside the driver.
- The phase margin is also contributed by the parasitic inductance of the LED wires from the LED anodes to OUT pins of the driver.

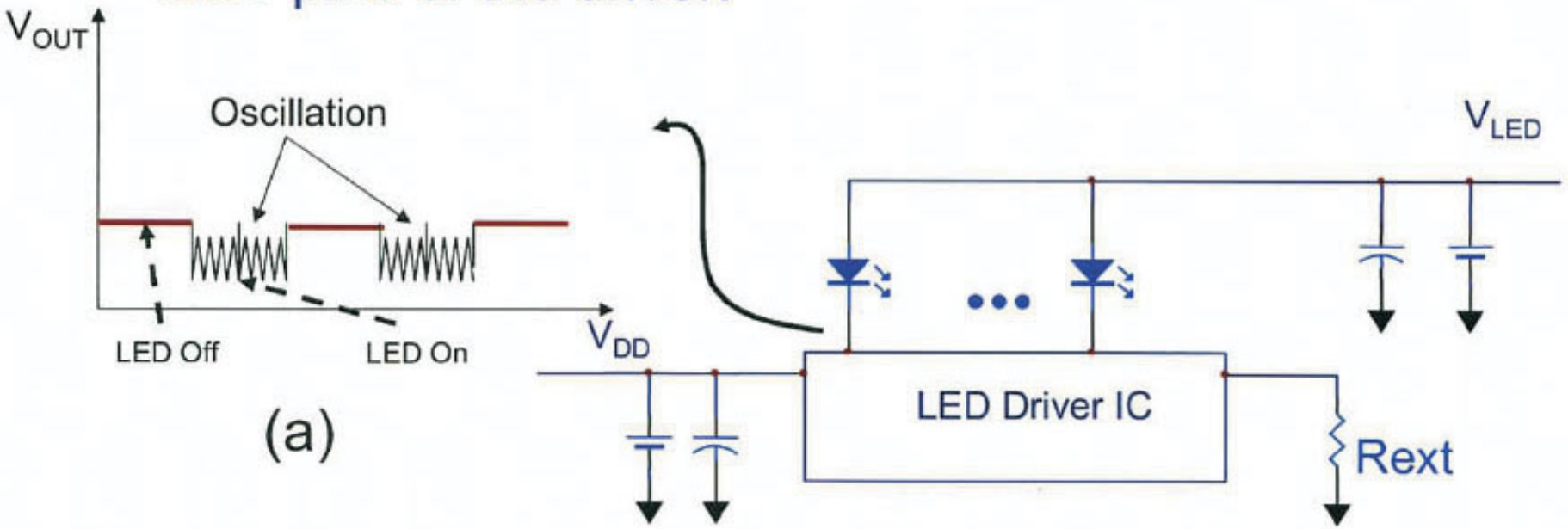


Fig. 27.

3.12 Vrext Oscillation

- The ill grounding of Rext will also has risks in output oscillation.
- Method to avoid oscillation in output port
  - Add Cext ≦ 47nF in shunt with pin Rext

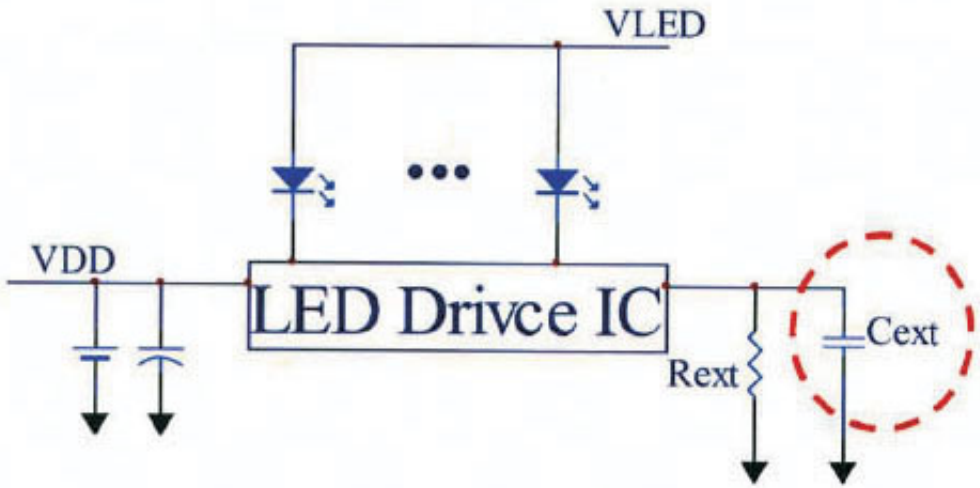


Fig. 28.

3.13 Power Supply's EMI Suppression

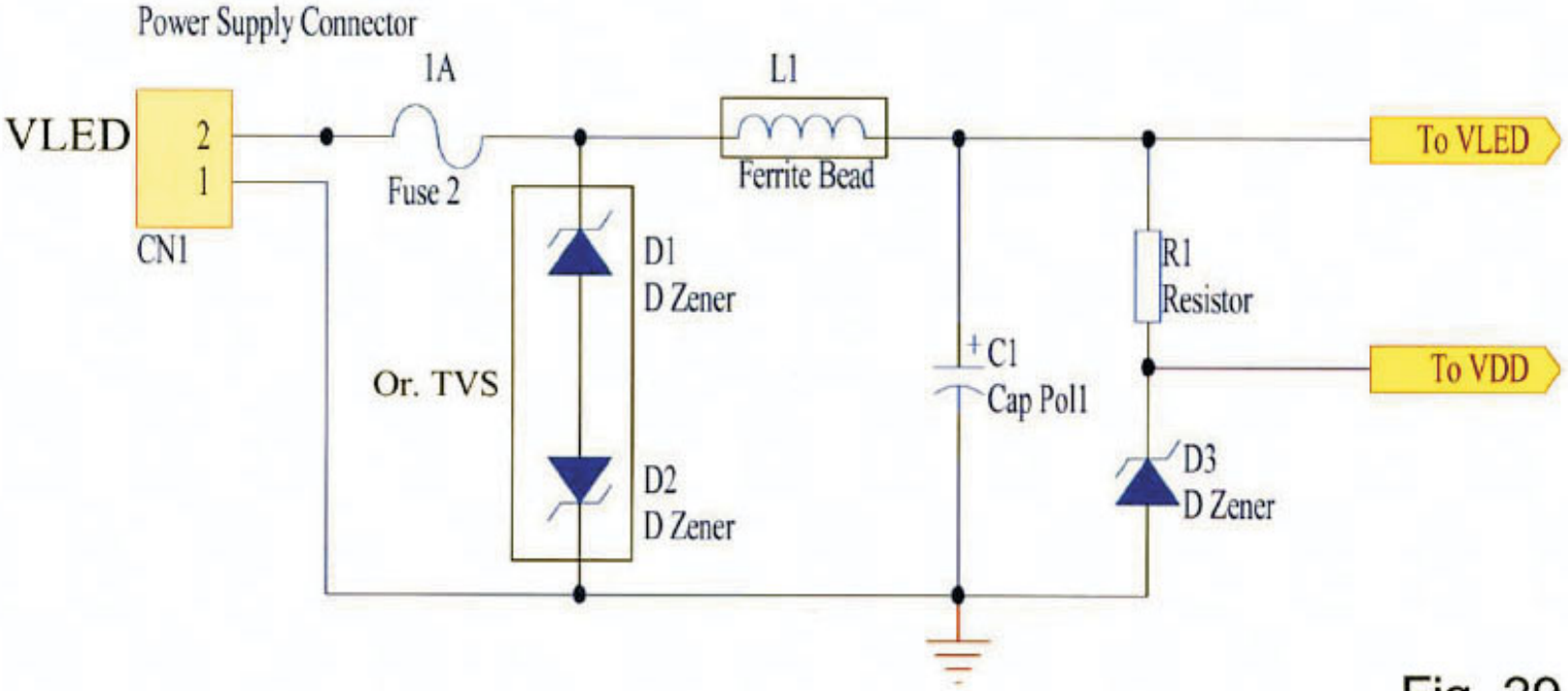
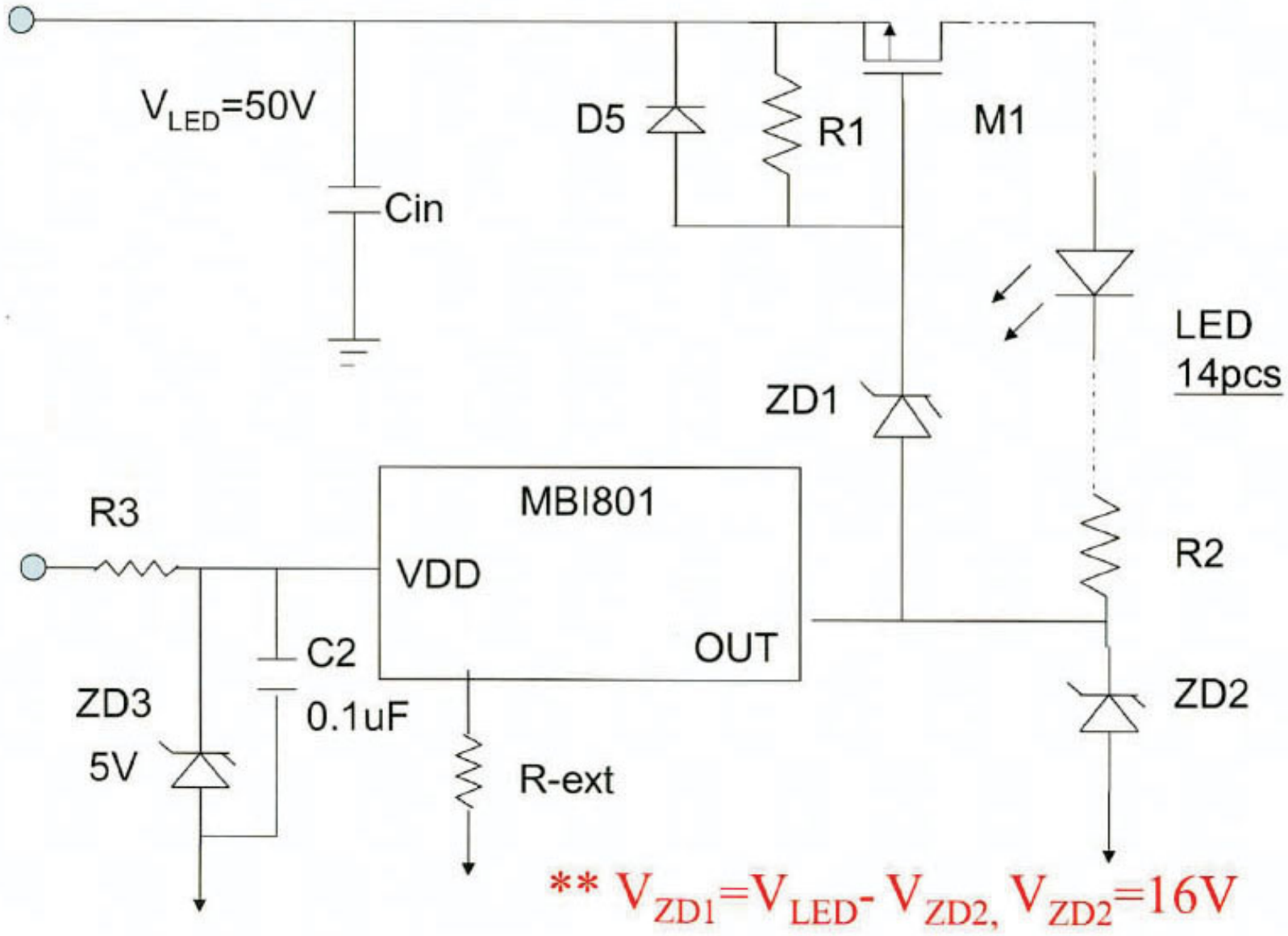


Fig. 29

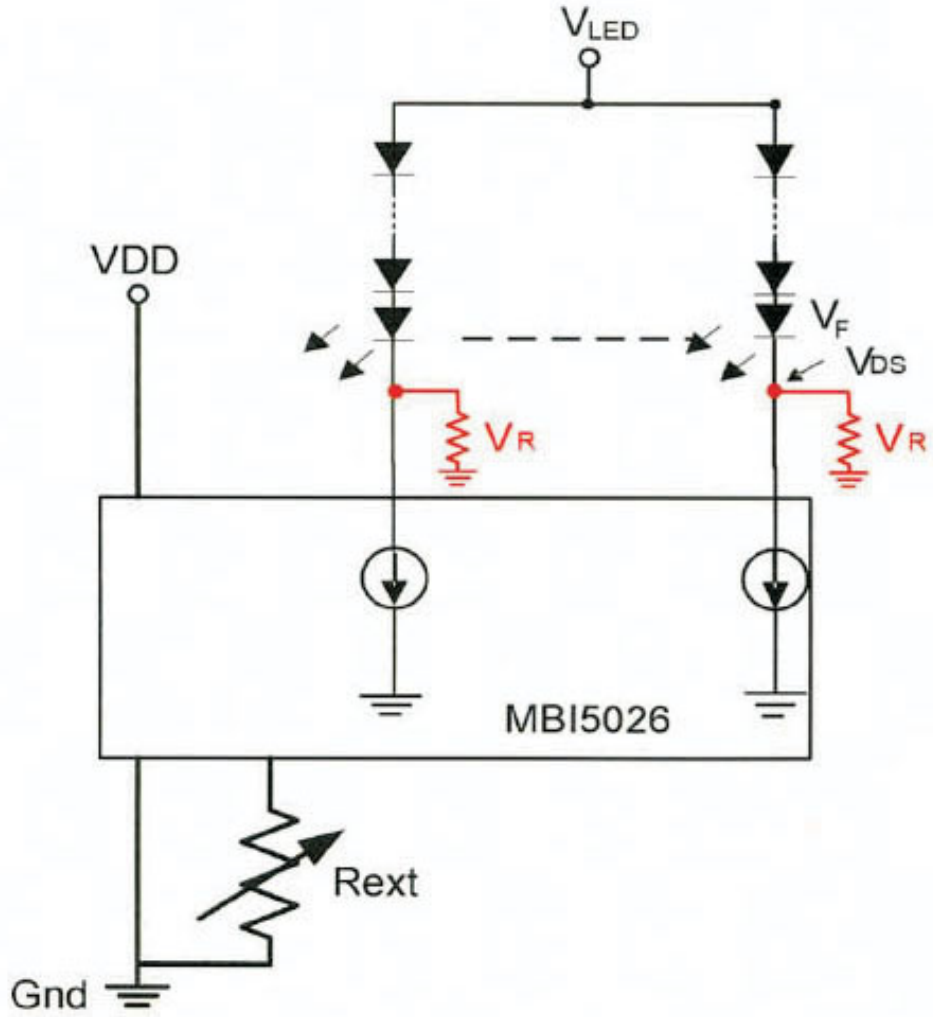
D1+D2: Total claim voltage =VLED +2V is recommended, or Bi-direction TVS component

Ferrite Bead : NiZn ferrite material is recommended

Applications of High Input Voltage-I



Applications of High Input Voltage-II



When output channels are turned off, most of supply voltage (VLED) will drop on VR.

Shunts a Mega Ohm resistance at output pin terminals to prevent LED from low Vf due to slight brightness.