Data Sheet: JN5139-001 and JN5139-Z01

IEEE802.15.4 and ZigBee Wireless Microcontrollers

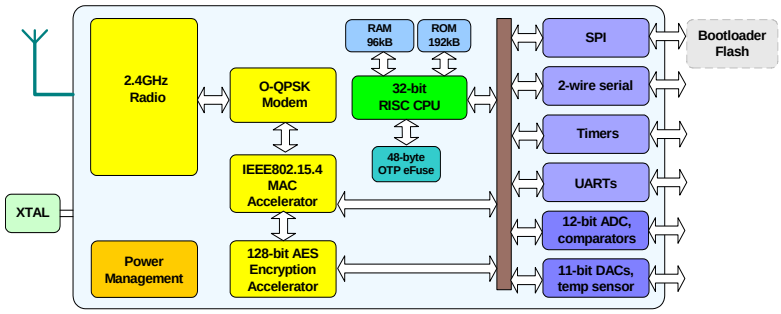
Overview

The JN5139 is a low power, low cost wireless microcontroller suitable for IEEE802.15.4 and ZigBee applications. The device integrates a 32-bit RISC processor, with a fully compliant 2.4GHz IEEE802.15.4 transceiver, 192kB of ROM, 96kB of RAM, and a rich mixture of analogue and digital peripherals.

The cost sensitive ROM/RAM architecture supports the storage of system software, including protocol stacks, routing tables and application code/data. An external flash memory may be used to store application code that will be bootloaded into internal RAM and executed at runtime.

The device integrates hardware MAC and AES encryption accelerators, power saving and timed sleep modes, and mechanisms for security key and program code encryption. These features all make for a highly efficient, low power, single chip wireless microcontroller for battery-powered applications.

Block Diagram



Benefits

- Single chip integrates transceiver and microcontroller for wireless sensor networks
- Cost sensitive ROM/RAM architecture, meets needs for volume application
- System BOM is low in component count and cost
- Hardware MAC ensures low power consumption and low processor overhead
- Extensive user peripherals

Applications

- Robust and secure low power wireless applications
- Wireless sensor networks, particularly IEEE802.15.4 and ZigBee systems
- Home and commercial building automation
- Remote Control
- Toys and gaming peripherals
- Industrial systems
- Telemetry and utilities (e.g. AMR)

Features: Transceiver

- 2.4GHz IEEE802.15.4 compliant
- 128-bit AES security processor
- MAC accelerator with packet formatting, CRCs, address check, auto-acks, timers
- Integrated power management and sleep oscillator for low power
- On-chip power regulation for 2.2V to 3.6V battery operation
- Deep sleep current 60nA
- Sleep current with active sleep timer 1.2µA
- Needs minimum of external components (< US$1 cost)
- Rx current 37mA
- Tx current 38mA
- Receiver sensitivity -97dBm
- Transmit power +3dBm

Features: Microcontroller

- 32-bit RISC processor sustains up to 16MIPs with low power
- 192kB ROM stores system firmware that includes Bootloader, and IEEE802.15.4 MAC
- 96kB RAM stores system data and bootloaded application code
- 48-byte OTP eFuse supporting AES based code encryption feature
- 4-input 12-bit ADC, 2 11-bit DACs, 2 comparators
- 2 Application timer/counters, 3 system timers
- 2 UARTs (one for debug)
- SPI port with 5 selects
- 2-wire serial interface
- Up to 21 DIO
- Pin compatible with JN5121

Industrial temperature range (-40°C to +85°C)

8x8mm 56-lead QFN

Lead-free and RoHS compliant

1 Introduction

The JN5139-001 and JN5139-Z01 are IEEE802.15.4 wireless microcontrollers that provide a fully integrated solution for applications using the IEEE802.15.4 and ZigBee standards in the 2.4 - 2.5GHz ISM frequency band [1]. They include all of the functionality required to meet the IEEE802.15.4 specification and have additional processor capability to run a wide range of applications including but not limited to Remote Control, Home and Building Automation, Toys and Gaming. The following table explains which software stack is compatible with which chip variant:

ROM Variant	802.15.4	JenNet	ZigBee 04
001	✓	✓	
Z01	✓	✓	✓

The devices include a Wireless Transceiver, RISC CPU, on-chip memory and an extensive range of peripherals.

Hereafter, the JN5139-001 and JN5139-Z01 will be referred to collectively as JN5139.

1.1 Wireless Microcontroller

Applications that transfer data wirelessly tend to be more complex than wired ones. Wireless protocols make stringent demands on frequencies, data formats, timing of data transfers, security and other issues. Application development must consider the requirements of the wireless network in addition to the product functionality and user interfaces. To minimise this complexity, Jennic provides a series of software libraries and interfaces that control the transceiver and peripherals of the JN5139. These libraries and interfaces remove the need for the developer to understand wireless protocols and greatly simplifies the programming complexities of power modes, interrupts and hardware functionality.

In view of the above, the register details of the JN5139 are not provided in the datasheet.

1.2 Wireless Transceiver

The Wireless Transceiver is highly integrated and, together with the integrated IEEE802.15.4 MAC library contained in ROM requires little knowledge of RF or wireless design.

The Wireless Transceiver comprises a low-IF 2.45GHz radio, an O-QPSK modem, a baseband controller and a security coprocessor. The radio has a 200Ω resistive differential antenna port that includes all the required matching components on-chip, allowing a differential antenna to be connected directly to the port, minimising the system BOM costs. Connection to a single ported antenna can be achieved using a 200/50Ω 2.45GHz balun. In addition, the radio also provides an output to control transmit-receive switching of external devices such as power amplifiers allowing applications that require increased transmit power to be realised very easily.

The Security coprocessor provides hardware-based 128-bit AES-CCM, CBC(1), CTR and CCM* processing as specified by the IEEE802.15.4 standard. It does this in-band on packets during transmission and reception, requiring minimal intervention from the CPU. It is also available for off-line use under software control for encrypting and decrypting packets generated by software layers and user applications. This means that these algorithms can be off-loaded by the CPU, increasing the processor bandwidth available for user applications.

The transceiver elements (radio, modem and baseband) work together to provide IEEE802.15.4 Medium Access Control under the control of a protocol stack.

(1) AES-CBC processing is only available off-line for use under software control.

1.3 RISC CPU and Memory

A 32-bit RISC CPU allows software to be run on-chip, its processing power being shared between the IEEE802.15.4 MAC protocol, other higher layer protocols and the user application. The JN5139 has a unified memory architecture, code memory, data memory, peripheral devices and I/O ports are organized within the same linear address space. The device contains 192kBytes of ROM, 96kBytes of RAM and a 48-byte OTP eFuse memory.

1.4 Peripherals

The following peripherals are available on-chip:

- Master SPI port with five select outputs
- Two UARTs
- Two programmable Timer/Counters with capture/compare facility
- Two programmable Sleep Timers and a Tick Timer
- Two-wire serial interface (compatible with SMbus and I^2C)
- Slave SPI port (shared with digital I/O)
- Twenty-one digital I/O lines (multiplexed with UARTs, timers and SPI selects)
- Four-channel, 12-bit, Analogue-to-Digital converter
- Two 11-bit Digital-to-Analogue converters
- Two programmable analogue comparators
- Internal temperature sensor and battery monitor

1.5 Block Diagram

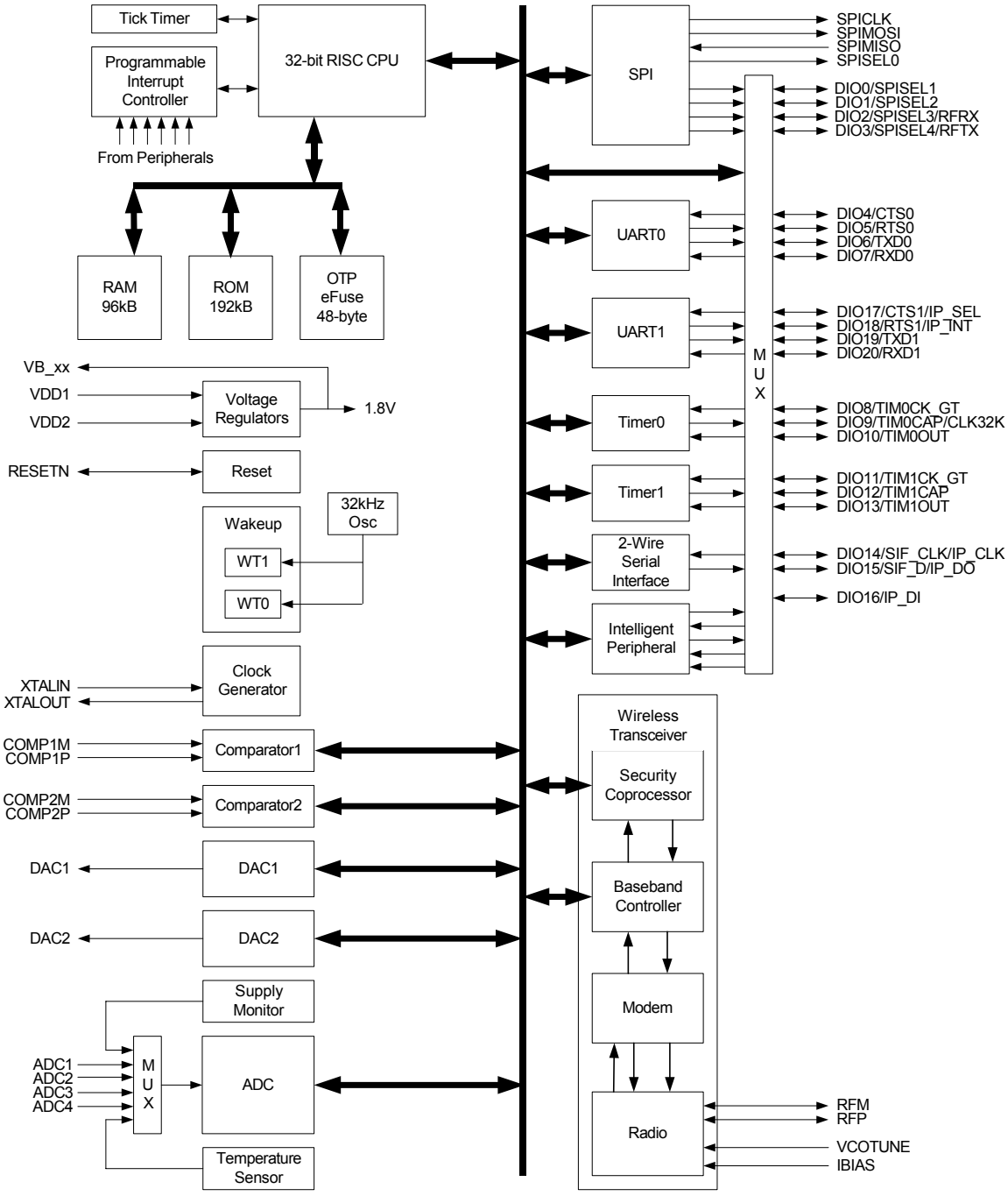


Figure 1: JN5139 Block Diagram

2 Pin Configurations

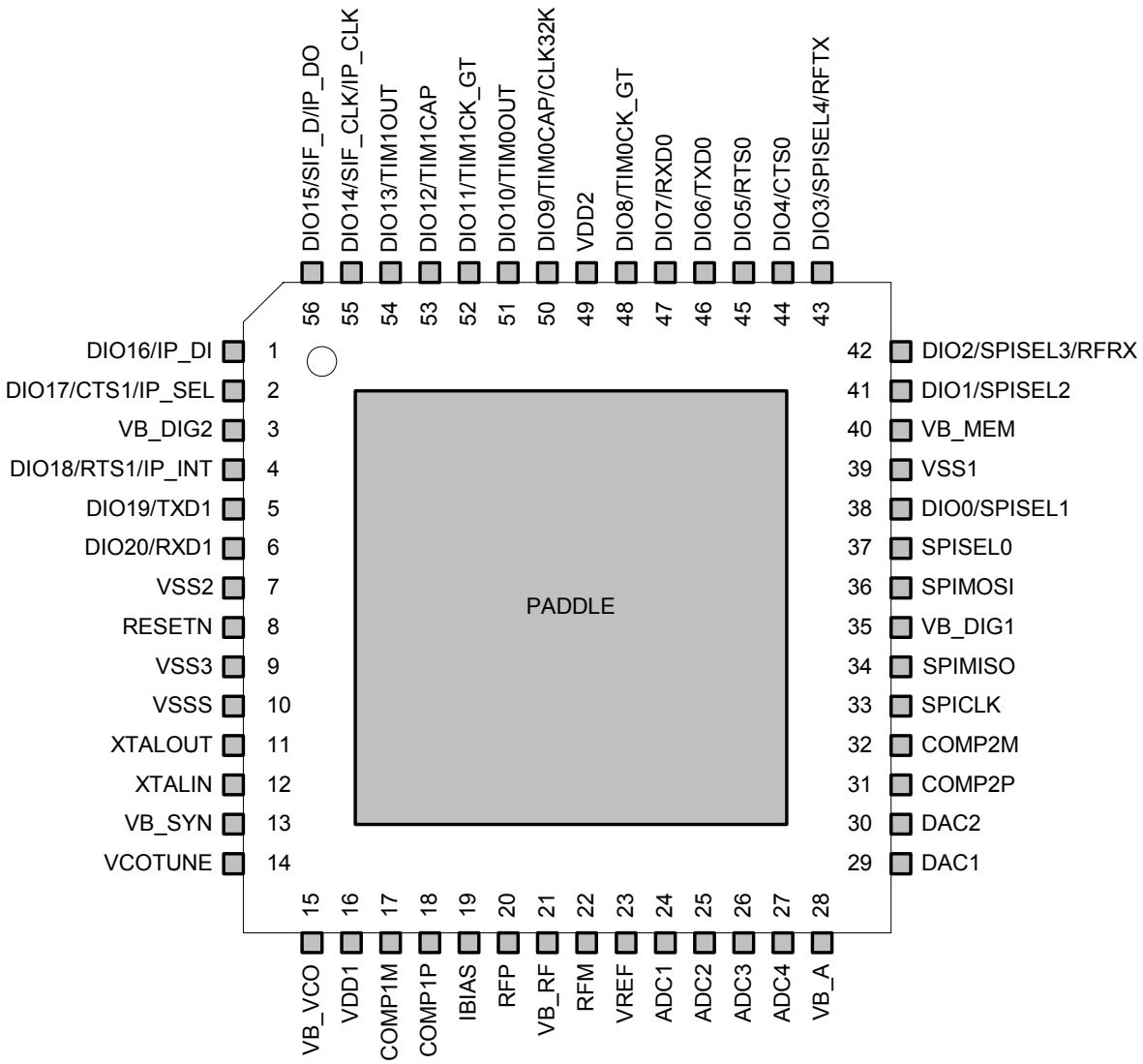


Figure 2: 56-pin QFN Configuration (top view)

Note: Please refer to Appendix B.3 for important applications information regarding the connection of the PADDLE to the PCB.

2.1 Pin Assignment

Pin No	Power supplies		Description
3, 13, 15, 21 28, 35, 40	VB_DIG2, VB_SYN, VB_VCO, VB_RF, VB_A, VB_DIG1, VB_MEM		Regulated supply voltage
16, 49	VDD1, VDD2		Device supplies: VDD1 for analogue, VDD2 for digital
7,9,10,39, PADDLE	VSS2, VSS3, VSSS, VSS1, VSSA		Device grounds
	General		
8	RESETN		Reset output/input
11, 12	XTALOUT, XTALIN		System crystal oscillator
	Radio		
14	VCOTUNE		VCO tuning RC network
19	IBIAS		Bias current control
20, 22	RFP, RFM		Differential antenna port
	Analogue Peripheral I/O		
24, 25, 26, 27	ADC1, ADC2, ADC3, ADC4		ADC inputs
23	VREF		Analogue peripheral reference voltage
29, 30	DAC1, DAC2		DAC outputs
17, 18, 31, 32	COMP1M, COMP1P, COMP2P, COMP2M		Comparator inputs
	Digital I/O		
	Function	**Alternate Function(s)**	
33	SPICLK		SPI Clock
36	SPIMOSI		SPI Master Out Slave In
34	SPIMISO		SPI Master In Slave Out
37	SPISEL0		SPI Slave Select Output 0
38	DIO0	SPISEL1	DIO0 or SPI Slave Select Output 1
41	DIO1	SPISEL2	DIO1 or SPI Slave Select Output 2
42	DIO2	SPISEL3, RFRX	DIO2 or SPI Slave Select Output 3 or Radio Receive Control Output
43	DIO3	SPISEL4, RFTX	DIO3 or SPI Slave Select Output 4 or Radio Transmit Control Output
44	DIO4	CTS0	DIO4 or UART 0 Clear To Send Input
45	DIO5	RTS0	DIO5 or UART 0 Request To Send Output
46	DIO6	TXD0	DIO6 or UART 0 Transmit Data Output
47	DIO7	RXD0	DIO7 or UART 0 Receive Data Input
48	DIO8	TIM0CK_GT	DIO8 or Timer0 Clock/Gate Input
50	DIO9	TIM0CAP,CLK32K	DIO9 or Timer0 Capture Input or CLK32K
51	DIO10	TIM0OUT	DIO10 or Timer0 PWM Output
52	DIO11	TIM1CK_GT	DIO11 or Timer1 Clock/Gate Input
53	DIO12	TIM1CAP, ADO	DIO12 or Timer1 Capture Input or Antenna Diversity Output
54	DIO13	TIM1OUT	DIO13 or Timer1 PWM Output
55	DIO14	SIF_CLK, IP_CLK	DIO14 or Serial Interface Clock or Intelligent Peripheral Clock Input
56	DIO15	SIF_D, IP_DO	DIO15 or Serial Interface Data or Intelligent Peripheral Data Out
1	DIO16	IP_DI	DIO16 or Intelligent Peripheral Data In
2	DIO17	CTS1, IP_SEL	DIO17 or UART 1 Clear To Send Input or Intelligent Peripheral Device Select Input
4	DIO18	RTS1, IP_INT	DIO18 or UART 1 Request To Send Output or Intelligent Peripheral Interrupt Output
5	DIO19	TXD1	DIO19 or UART 1 Transmit Data Output
6	DIO20	RXD1	DIO20 or UART 1 Receive Data Input

2.2 Pin Descriptions

2.2.1 Power Supplies

The device is powered from the VDD1 and VDD2 pins, each being decoupled with a 100nF ceramic capacitor. VDD1 is the power supply to the analogue circuitry; it should be decoupled to ground. VDD2 is the power supply for the digital circuitry; it should be decoupled to ground. A 10uF tantalum capacitor is required at the common ground star point of analogue and digital supplies. Decoupling pins for the internal 1.8V regulators are provided which require a 100nF capacitor located as close to the device as practical. VB_VCO, VB_RF, VB_A and VB_SYN should be decoupled to analogue ground, while VB_MEM, VB_DIG1 and VB_DIG2 should be decoupled to ground. VB_SYN and VB_RF also require an additional 47pF capacitor. See also Appendix B for connection details.

VSSA is the analogue ground, connected to the paddle of the device, while VSSS, VSS1, VSS2, VSS3 are digital ground pins. All grounds should be connected to a ground plane.

2.2.2 Reset

RESETN is a bi-directional active low reset pin that is connected to a 40kΩ internal pull-up resistor. It may be pulled low by an external circuit, or can be driven low by the JN5139 if an internal reset is generated. Typically, it will be used to provide a system reset signal. Refer to section 6.2, External Reset, for more details.

2.2.3 16MHz System Clock

A crystal connected between XTALIN and XTALOUT drives the system clock. A capacitor to analogue ground is required on each of these pins. Refer to section 5.1 16MHz System Clock / Crystal Oscillator for more details.

2.2.4 Radio

A 200Ω balanced antenna (such as a printed circuit antenna) can be connected directly to the radio interface pins RFM and RFP.

A single-ended 50Ω antenna such as a ceramic type or SMA connector for an external antenna requires the addition of a 200/50Ω 2.45GHz balun transformer connected to the antenna pins. The balun differential port should be connected to the antenna port with 200Ω balanced controlled impedance track. A 50Ω controlled impedance track should be used to connect the unbalanced port of the balun to the antenna to ensure good impedance matching and reduce losses and reflections.

A simple external loop filter circuit consisting of two capacitors and a resistor is connected to VCOTUNE. Refer to section 8.1 Radio for more details.

An external resistor (43kΩ) is required between IBIAS and analogue ground to set various bias currents and references within the radio.

2.2.5 Analogue Peripherals

Several of the analogue peripherals require a reference voltage to use as part of their operations. They can use either an internal reference voltage or an external reference connected to VREF. This voltage is referenced to analogue ground and the performance of the analogue peripherals is dependant on the quality of this reference.

There are four ADC inputs, two pairs of comparator inputs and two DAC outputs. The analogue I/O pins on the JN5139 can have signals applied up to 0.3v higher than VDD1. A schematic view of the analogue I/O cell is shown in Figure 3: Analogue I/O Cell

In reset and deep sleep, the analogue peripherals are all off and the DAC outputs are in a high impedance state.

In sleep, the ADC and DACs are off, with the DAC outputs in high impedance state. The comparators may optionally be used as a wakeup source.

Unused ADC and comparator inputs should be left unconnected.

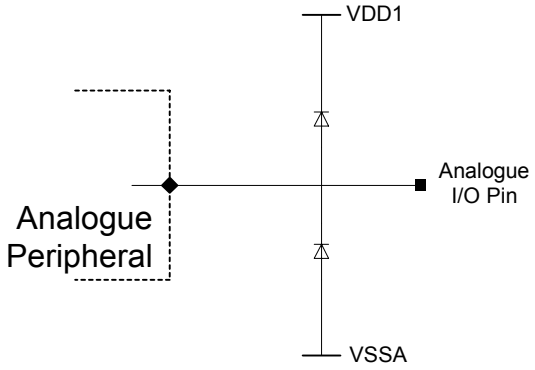


Figure 3: Analogue I/O Cell

2.2.6 Digital Input/Output

Digital I/O pins on the JN5139 can have signals applied up to 2V higher than VDD2 (with the exception of pins DIO9 and DIO10 that are 3V tolerant) and are therefore TTL-compatible with VDD2 > 3V. For other DC properties of these pins see section 17.2.3 I/O Characteristics.

When used in their primary function all Digital Input/Output pins are bi-directional and are connected to weak internal pull up resistors (40kΩ nominal) that can be disabled. When used in their secondary function (selected when the appropriate peripheral block is enabled through software library calls) then their direction is fixed by the function. The pull up resistor is enabled or disabled independently of the function and direction; the default state from reset is enabled.

A schematic view of the digital I/O cell is in Figure 4: DIO Pin Equivalent Schematic.

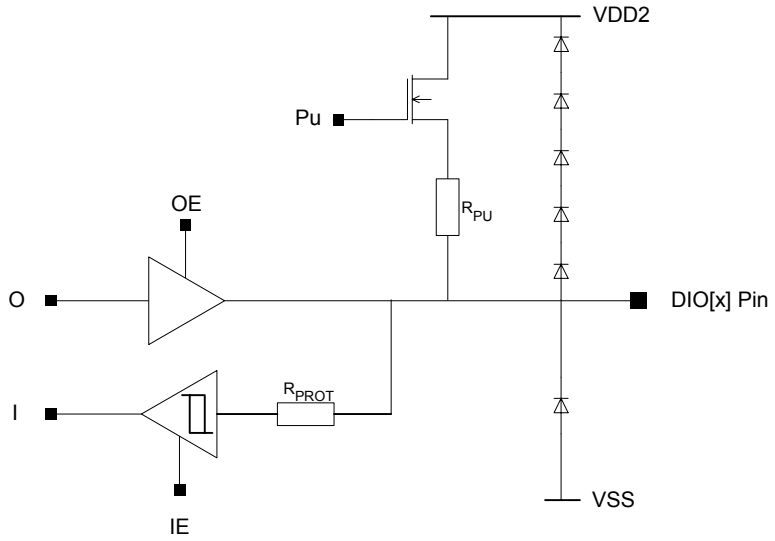


Figure 4: DIO Pin Equivalent Schematic

In reset, the digital peripherals are all off and the DIO pins are set as high-impedance inputs. During sleep and deep sleep, the DIO pins retain both their input/output state and output level that was set as sleep commences. If the DIO pins were enabled as inputs and the interrupts were enabled then these pins may be used to wake up the JN5139 from sleep.

3 CPU

The CPU of the JN5139 is a 32-bit load and store RISC processor. It has been architected for three key requirements:

- Low power consumption for battery powered applications
- High performance to implement a wireless protocol at the same time as complex applications
- Efficient coding of high-level languages such as C provided with the Jennic Software Developers Kit

It features a linear 32-bit logical address space with unified memory architecture, accessing both code and data in the same address space. Registers for peripheral units, such as the timers, UARTs and the baseband processor are also mapped into this space.

The CPU contains a block of 32 32-bit General-Purpose (GP) registers together with a small number of special purpose registers which are used to store processor state and control interrupt handling. The contents of any GP register can be loaded from or stored to memory, while arithmetic and logical operations, shift and rotate operations, and signed and unsigned comparisons can be performed either between two registers and stored in a third, or between registers and a constant carried in the instruction. Operations between general or special-purpose registers execute in one cycle (16MHz) while those that access memory require a further cycle to allow the memory to respond.

The instruction set manipulates 8, 16 and 32-bit data, stored in big-endian format; this means that programs can use objects of these sizes very efficiently. Manipulation of 32-bit quantities is particularly useful for protocols and high-end applications allowing algorithms to be implemented in fewer instructions than on smaller word-size processors, and to execute in fewer clock cycles.

The instruction set is designed for the efficient implementation of high-level languages such as C. Access to fields in complex data structures is very efficient due to the provision of several addressing modes, together with the ability to be able to use any of the GP registers to contain the address of objects. Subroutine parameter passing is also made more efficient by using GP registers rather than pushing objects on the stack. The recommended programming method for the JN5139 is by using C, which is supported by a software developer kit comprising a C compiler, linker and debugger.

The CPU architecture also contains features that make the processor suitable for embedded, real-time applications. In some applications, it may be necessary to use a real-time operating system to allow multiple tasks to run on the processor.

Embedded applications require efficient handling of external hardware events. Exception processing (including reset and interrupt handling) is enhanced by the inclusion of a number of special-purpose registers into which the PC and status register contents are copied as part of the operation of the exception hardware. This means that the essential registers for exception handling are stored in one cycle, rather than the slower method of pushing them onto the processor stack. The PC is also loaded with the vector address for the exception that occurred, allowing the handler to start executing in the next cycle.

To improve power consumption a number of power-saving modes are implemented in the JN5139, described more fully in section 16 - Power Management and Sleep Modes. One of these modes is the CPU doze mode; under software control, the processor can be shut down and on an interrupt will wake up to service the request.

4 Memory Organisation

This section describes the different memories found within the JN5139. The device contains ROM, RAM, OTP eFuse memory, the wireless transceiver and peripherals all within the same linear address space.

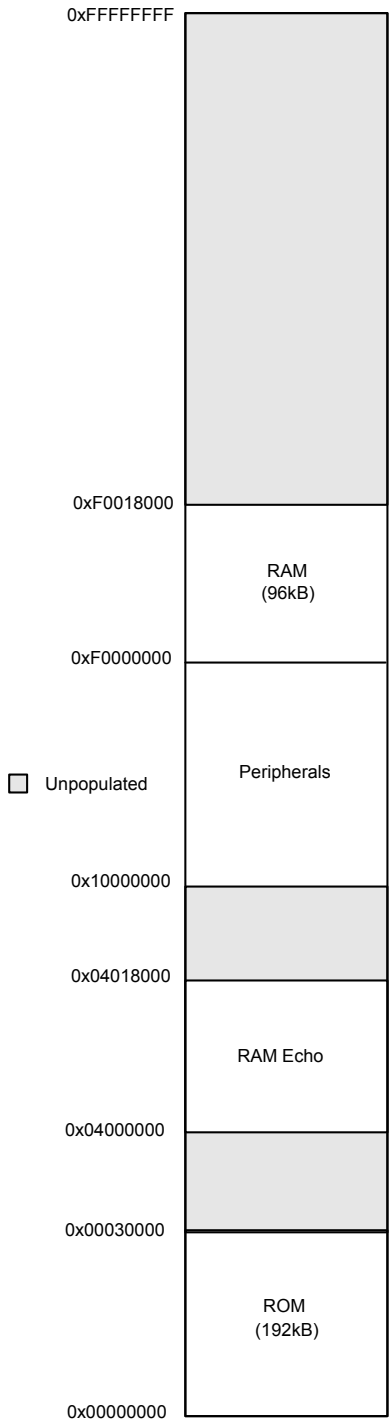


Figure 5: JN5139 Memory Map

4.1 ROM

The ROM is 192K bytes in size, organized as 48k x 32-bit words and can be accessed by the CPU in a single clock cycle. The ROM contents include bootloader to allow external Flash memory contents to be bootloaded into RAM at runtime, a default interrupt vector table, an interrupt manager, IEEE802.15.4 MAC and assorted APIs for interfacing to the MAC and on-chip hardware peripherals. The operation of the boot loader is described in detail in Application Note JN-AN-1003 Boot Loader Operation [2]. The interrupt manager routes interrupt calls to the application's soft interrupt vector table contained within RAM. Section 7 contains further information regarding the handling of interrupts. Typical ROM contents are shown in Figure 6.

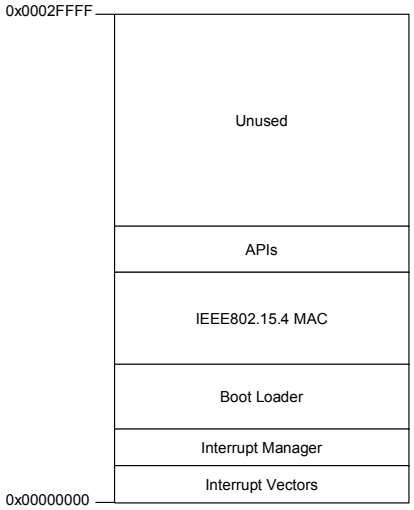


Figure 6: ROM contents

4.2 RAM

The JN5139 contains 96k bytes of high speed RAM organized as 24k x 32-bit. It can be used for both code and data storage and is accessed by the CPU in a single clock cycle. At reset, a boot loader controls the loading of segments of code and data from an external memory connected to the SPI port, into RAM. Software can control the power supply to the RAM allowing the contents to be maintained during a sleep period when other parts of the device are un-powered. Typical RAM contents are shown in Figure 7.

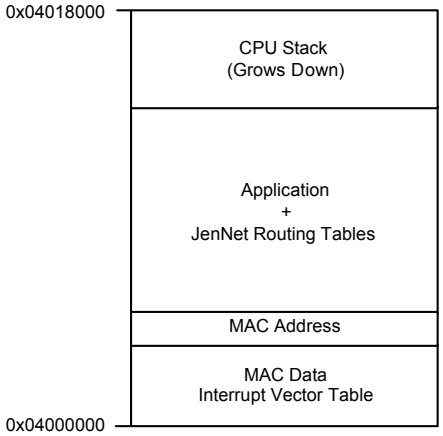


Figure 7: Typical RAM Contents

4.3 OTP eFuse Memory

The JN5139 contains 48-bytes of eFuse memory; this is one time programmable memory that is organised as 12 x 32-bit words, 4 words are reserved by Jennic and 4 words are reserved for future use. The remaining 4 words are fully user programmable, designed to allow for the storage of a 128-bit encryption key for secure external memory encryption (see section 4.4.1)

For full details on how to program and use the eFuse memory, please refer to application note JN-AN-1062 Using OTP eFuse Memory [3].

Alternatively, Jennic can provide an eFuse programming service for customers that wish to use the eFuse but do not wish to undertake this for themselves. For further details of this service, please contact your local Jennic sales office.

4.4 External Memory

An external memory with an SPI interface may be used to provide storage for program code and data for the device when external power is removed. The memory is connected to the SPI interface using select line SPISEL0; this select line is dedicated to the external memory interface and is not available for use with other external devices. See Figure 8 for connection details.

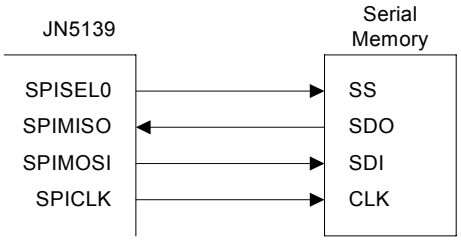


Figure 8: Connecting External Serial Memory

At reset, the contents of this memory are copied into RAM by the software boot loader. The Flash memory devices that are supported as standard through the JN5139 bootloader are given in Table 1. Jennic recommends that where possible one of these devices should be selected.

Manufacturer	Device Number
SST (Silicon Storage Technology)	25VF010A (1Mbyte device)
Numonyx	M25P10-A (1Mbyte device), M25P40 (4Mbyte device)

Table 1: Supported Flash Memories

Applications wishing to use an alternate Flash memory device should refer to application note JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader [4]. This application note provides guidance on developing an interface to an alternate device.

4.4.1 External Memory Encryption

The contents of the external serial memory can be encrypted. The AES security processor combined with a user programmable 128-bit encryption key is used to encrypt the contents of the external memory. The encryption key is stored in eFuse.

When bootloading program code from external serial memory, the JN5139 automatically accesses the encryption key to execute the decryption process. User program code does not need to handle any of the decryption process; it is a transparent process.

With encryption enabled, the time taken to boot code from external Flash memory is increased.

4.5 Peripherals

All peripherals have their registers mapped into the memory space. Access to these registers requires 3 clock cycles. Applications have access to the peripherals through the software libraries that present a high-level view of the peripheral's functions through a series of dedicated software routines. These routines provide both a tested method for using the peripherals and allow bug-free application code to be developed more rapidly. For details, see the Integrated Peripherals API Reference Manual (JN-RM-2001).

4.6 Unused Memory Addresses

Any attempt to access an unpopulated memory area will result in a bus error exception (interrupt) being generated.

5 System Clocks

Two system clocks are used to provide timing references into the on-chip subsystems of the JN5139. A 16MHz clock, generated by a crystal-controlled 16MHz oscillator, is used by the transceiver, processor, memory and digital and analogue peripherals. A 32kHz clock is used by the sleep timer and during the startup phase of the chip.

5.1 16MHz System Clock / Crystal Oscillator

The JN5139 contains the necessary on-chip components to build a 16 MHz reference oscillator with the addition of an external crystal resonator, two tuning capacitors and a resistor. The schematic of these components are shown in Figure 9. The two capacitors, C1 and C2, will typically be 15pF ±5% and use a COG dielectric, R2 should be 1M5Ω. Due to the small size of the capacitors, it is important to keep the traces to the external components as short as possible. The on-chip transconductance amplifier is compensated for temperature variation, and is self-biasing by means of the internal resistor R1. The electrical specification of the oscillator can be found in section 17.3.7. For detailed application support and specification of the crystal required and factors affecting C1 and C2 see Appendix B.1.

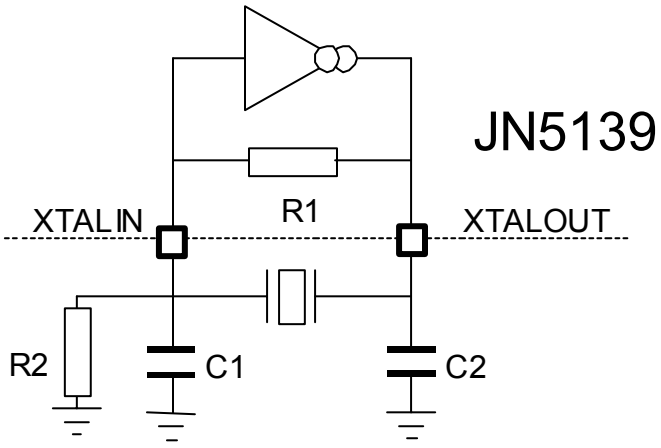


Figure 9: Crystal oscillator connections

The clock generated by this oscillator provides the reference for most of the JN5139 subsystems, including the transceiver, processor, memory and digital and analogue peripherals.

5.2 32kHz System Clock

The 32kHz system clock is used for timing the length of a sleep period (see section 16 Power Management and Sleep Modes) and also to generate the system clock used internally during reset. The clock can be selected from one of two sources through the application software:

- 32kHz RC Oscillator
- 32kHz External Clock

Once a clock source has been selected, then it will remain in use for all 32kHz timing until a chip reset is performed. Upon a chip reset the JN5139 defaults to using the internal 32kHz RC Oscillator.

5.2.1 32kHz RC Oscillator

The internal 32kHz RC oscillator is the default clock and requires no external components. It provides a low speed clock for use in sleep mode. The internal timing components of the oscillator have a wide tolerance due to manufacturing process variation and so the oscillator runs nominally at 32kHz ±30%. To make this useful as a timing source for accurate wakeup from sleep, a frequency calibration factor derived from the more accurate 16MHz clock may be applied. The calibration factor is derived through software, details can be found in section 12.3.1. For detailed electrical specifications, see section 17.3.6.

5.2.2 32kHz External Clock

An externally supplied 32kHz reference clock on the CLK32K input (DIO9) may be provided to the JN5139. This would allow the 32kHz system clock to be sourced from a very stable external oscillator module, allowing more accurate sleep cycle timings. (See section 17.2.3 I/O Characteristics, DIO9 is a 3V tolerant input)

6 Reset

A system reset initialises the device to a predefined state and forces the CPU to start program execution from the reset vector. The reset process that the JN5139 goes through is as follows.

When power is applied, the internal 32kHz oscillator starts up and stabilises, which takes approximately 100μsec. At this point, the 16MHz crystal oscillator is enabled and power is applied to the processor and digital logic. The logic blocks are held in reset until the 16MHz crystal oscillator stabilises, which typically takes 2.75ms.

Once the oscillator is up and running the internal reset is removed from the CPU and peripheral logic and the CPU starts to run code beginning at the reset vector, consisting of initialisation code and the resident Boot Loader (described in JN-AN-1003 Boot Loader Operation [2]).

Section 17.3.1 provides detailed electrical data and timing.

The JN5139 has three sources of reset:

- Internal Power-on Reset
- External Reset
- Software Reset

Note: When the device exits a reset condition, device operating parameters (voltage, frequency, temperature, etc.) must be met to ensure operation. If these conditions are not met, then the device must be held in reset until the operating conditions are met. (See section 17.3.1)

When reset is low, the digital logic and RAM are not powered and therefore anything stored in the RAM after reset is released cannot be guaranteed to still be valid.

6.1 Internal Power-on Reset

For the majority of applications the internal power-on reset is capable of generating the required reset signal. When power is applied to the device, the power-on reset circuit monitors the rise of the VDD supply. When VDD reaches the specified threshold, the reset signal is generated and can be observed as a rising edge on the RESETN pin. This signal is held internally until the power supply and oscillator stabilisation time has elapsed, at which point the internal reset signal is then removed and the CPU is allowed to run.

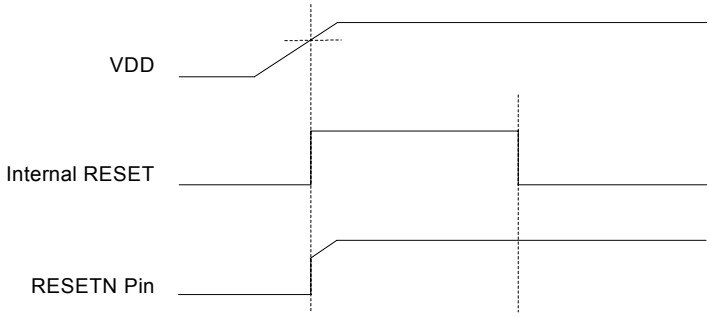


Figure 10: Internal Power-on Reset

The external resistor and capacitor provides a simple reset operation when connected to the RESETN pin, as shown in Figure 11. This can be used to extend the reset length and help in systems with noisy reset push-buttons.

If the application requires a power supply reset to be used, i.e. removing and then applying VDD, it is important that the device decoupling capacitors are completely discharged (less than 0.4v) before the VDD is re-applied. Failure to do so may inhibit device operation. If complete discharge is difficult to achieve then it is recommended to use of an external reset device to hold the device in reset whilst the voltage has dropped below the device operating voltage range.

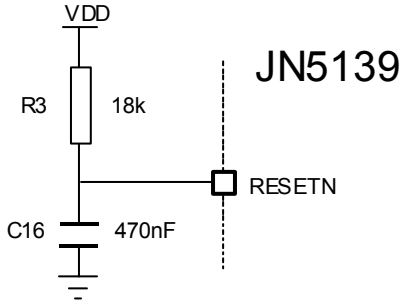


Figure 11: External Reset Generation

6.2 External Reset

An external reset is generated by a low level on the RESETN pin. Reset pulses longer than the minimum pulse width will generate a reset during active or sleep modes. Shorter pulses are not guaranteed to generate a reset. The JN5139 is held in reset while the RESETN pin is low and when the applied signal reaches the Reset Threshold Voltage (V_{RST}) on its positive edge, the internal reset process starts.

Multiple devices may connect to the RESETN pin in an open-collector mode. The JN5139 has an internal pull-up resistor although an external pull-up resistor is recommended when multiple devices connect to the RESETN pin. The pin is an input for an external reset and an output, driven low, during the power-on reset and software reset. No devices should drive the RESETN pin high.

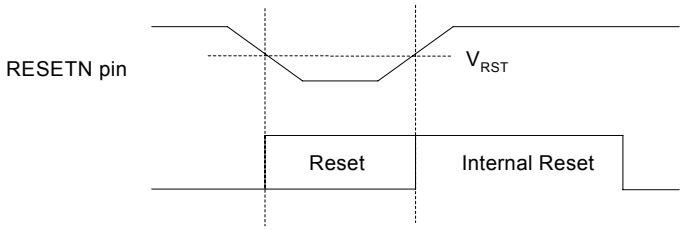


Figure 12: External Reset

6.3 Software Reset

A system reset can be triggered at any time through software control, causing a full chip reset and invalidating the RAM contents. For example this can be executed within a user's application upon detection of a system failure. When performing the reset, the RESETN pin is driven low for 1µsec; depending on the external components this may or may not be visible on the pin.

In addition, the RESETN line can be driven low by the JN5139 to provide a reset to other devices in the system (e.g. external sensors) without resetting itself. When the RESETN line is not driven it will pull back high through either the internal pull-up resistor or any external circuitry. It is essential to ensure that the RESETN line pulls back high within 100µsec after the JN5139 stops driving the line; otherwise a system reset will occur. Due to this, careful consideration should be taken of any capacitance on this line. For instance, the RC values recommended in section 6.1 may need to be replaced with a suitable reset IC.

7 Interrupt System

The interrupt system on the JN5139 is a hardware-vectored interrupt system. The JN5139 provides several interrupt sources, some associated with CPU operations (CPU exceptions) and others which are used by hardware in the device. When an interrupt occurs the CPU stops executing the current program and loads its program counter with a fixed hardware address specific to that interrupt. The interrupt handler or interrupt service routine is stored at this location and is run on the next CPU cycle. Execution of interrupt service routines is always performed in supervisor mode. Interrupt sources and their vector locations are listed in Table 2 below:

Interrupt Source	Vector Location	Interrupt Definition
Reset	0x100	Software or hardware reset
Bus Error	0x200	Bus error or attempt to access invalid physical address
Tick Timer	0x500	Tick Timer expiry
Alignment	0x600	Load/Store to naturally not aligned location
Illegal Instruction	0x700	Illegal instruction in instruction stream
Hardware Interrupts	0x800	Hardware Interrupt
System Call	0xC00	System Call Initiated by software (l.sys instruction)
Trap	0xE00	Caused by l.trap instruction

Table 2: Interrupt Vectors

7.1 System Calls

Executing the `l.sys` instruction causes a system call interrupt to be generated. The purpose of this interrupt is to allow a task to switch into supervisor mode when a real time operating system is in use, see section 3 for further details. It also allows a software interrupt to be issued, as does execution of the `l.trap` instruction.

7.2 Processor Exceptions

7.2.1 Bus Error

A bus error exception is generated when software attempts to access a memory address that does not exist, or is not populated with memory or peripheral registers.

7.2.2 Alignment

Alignment exceptions are generated when software attempts to access objects that are not aligned to natural word boundaries. 16-bit objects must be stored on even byte boundaries, while 32-bit objects must be stored on quad byte boundaries. For instance, attempting to read a 16-bit object from address 0xFFF1 will trigger an alignment exception as will a read of a 32-bit object from 0xFFF1, 0xFFF2 or 0xFFF3. Examples of legal 32-bit object addresses are 0xFFF0, 0xFFF4, 0xFFF8 etc.

7.2.3 Illegal Instruction

If the CPU reads an unrecognised instruction from memory as part of its instruction fetch, it will cause an illegal instruction exception.

7.3 Hardware Interrupts

Hardware interrupts generated from the transceiver, analogue or digital peripherals and DIO pins are individually masked using the Programmable Interrupt Controller (PIC). Management of interrupts is provided in the peripherals library. Further details of interrupts are provided for the functions in their respective sections in this datasheet.

Interrupts are used to wake the JN5139 from sleep. The peripherals, baseband controller, security coprocessor and PIC are powered down during sleep but the DIO interrupts and optionally the wake-up timers and analogue comparator interrupts remain powered to bring the JN5139 out of sleep.

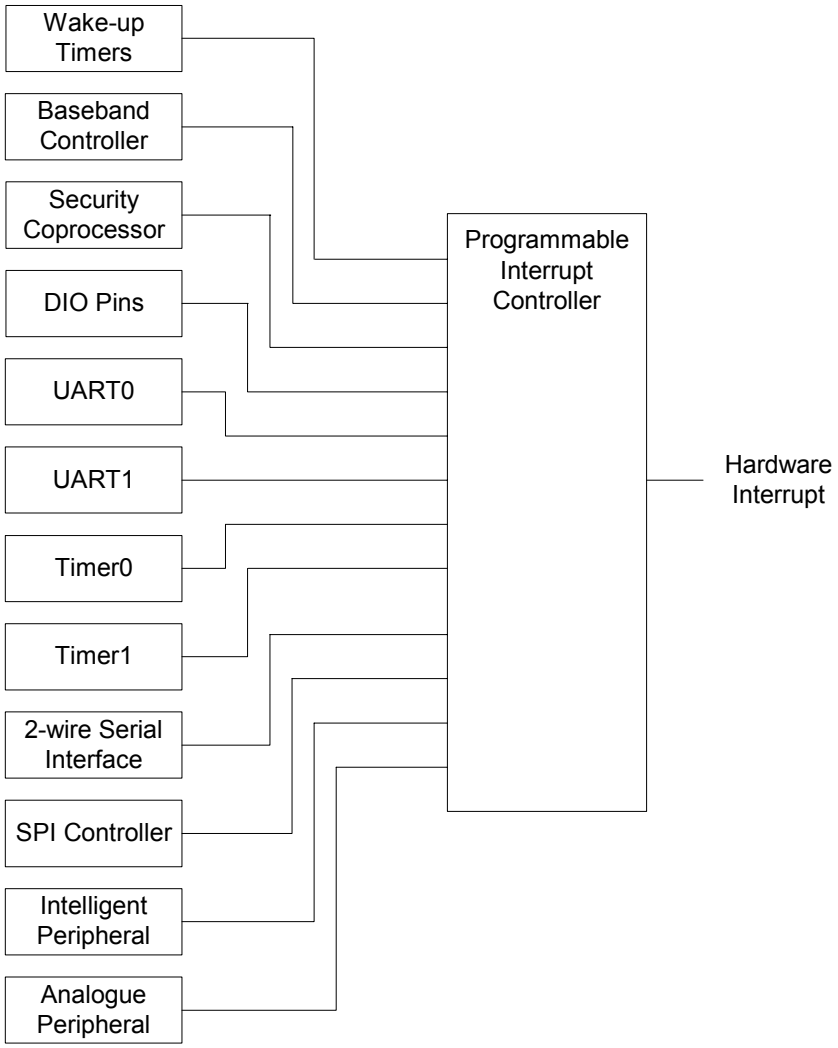


Figure 13: Programmable Interrupt Controller

8 Wireless Transceiver

The wireless transceiver comprises a 2.45GHz radio, an O-QPSK modem, a baseband processor, a security coprocessor and PHY controller. These blocks, with protocol software provided as a library, implement an IEEE802.15.4 standards-based wireless transceiver that transmits and receives data over the air in the unlicensed 2.4GHz band.

8.1 Radio

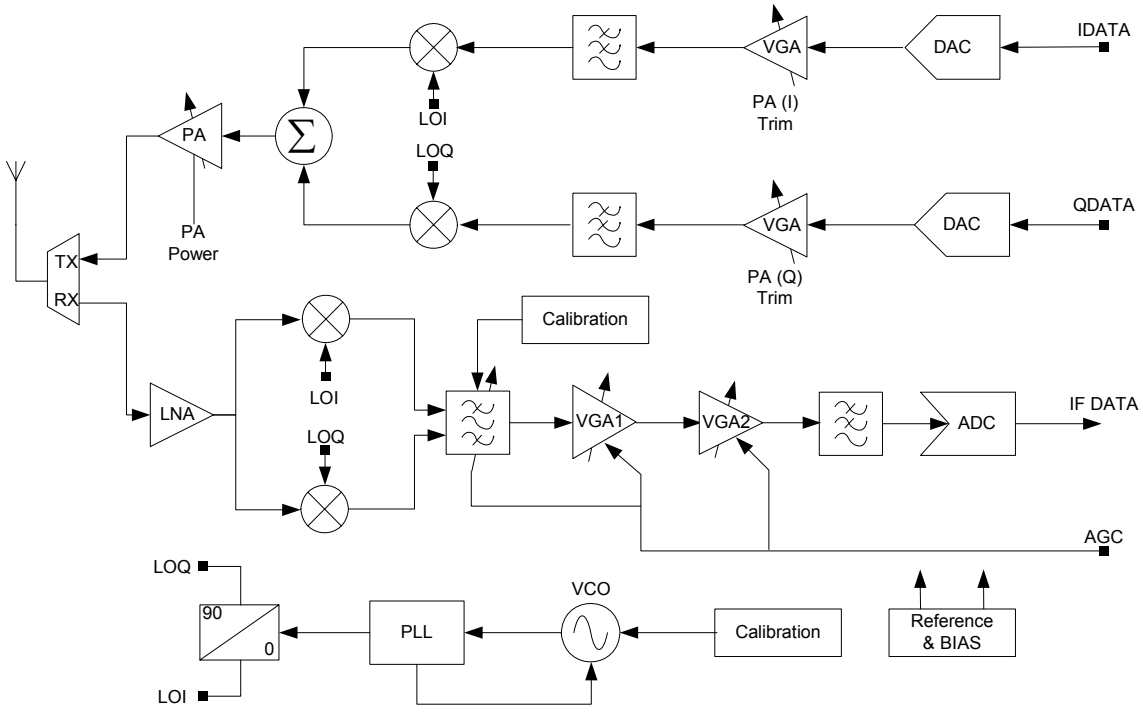


Figure 14: Radio Architecture

The radio comprises a low-IF receive path and a direct up-conversion transmit path, which converge at the TX/RX switch. This switch includes the necessary matching components such that a 200Ω differential antenna may be directly connected without external components. Alternatively, a balun can be used for single ended antennas.

The 16MHz crystal oscillator feeds a divider, which provides the frequency synthesiser with a reference frequency. The synthesiser contains programmable feedback dividers, phase detector, charge pump and internal Voltage Controlled Oscillator (VCO). The VCO has no external components, and includes calibration circuitry to compensate for differences in internal component values due to process and temperature variations. The VCO is controlled by a Phase Locked Loop (PLL) that has a loop filter comprising 3 external components. A programmable charge pump is also used to tune the loop characteristic. Finally, quadrature (I and Q) local oscillator signals for the mixer drives are derived.

The receiver chain starts with the low noise amplifier / mixer combination whose outputs are passed to the polyphase bandpass filter. This filter provides the channel definition as well as image frequency rejection. The signal is then passed to two variable gain amplifier blocks. The gain control for these stages and the bandpass filter is derived in the automatic gain control (AGC) block within the Modem. The signal is conditioned with the anti-alias low pass filter before being converted to a digital signal with a flash ADC.

In the transmit direction, the digital I and Q streams from the Modem are passed to I and Q quadrature DAC blocks which are buffered and low-pass filtered, before being applied to the modulator mixers. The summed 2.4 GHz signal is then passed to the RF Power Amplifier (PA), whose power control can be selected from one of six settings. The output of the PA drives the antenna via the RX/TX switch.

8.1.1 Radio External components

The VCO loop filter requires three external components and the IBIAS pin requires one external component as shown in Figure 15. These components should be placed close to the JN5139 pins and analogue ground.

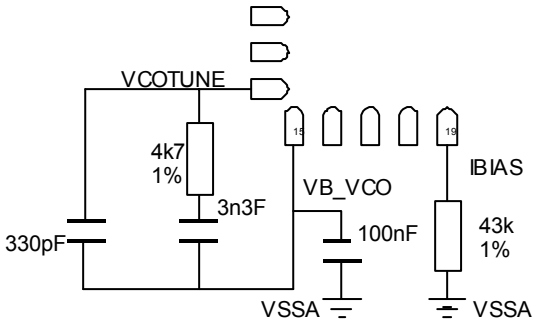


Figure 15: VCO Loop Filter and IBIAS

The radio is powered from a number of internal 1.8V regulators fed from the analogue supply VDD1, in order to provide good noise isolation between the digital logic of the JN5139 and the analogue blocks. These regulators are also controlled by the baseband controller and protocol software to minimise power consumption. Decoupling for internal regulators is required as described in section 2.2.1, Power Supplies.

In addition, as described in section 8.1, for single ended antennas or connectors a balun will be required.

8.1.2 Antenna Diversity

Support is provided for antenna diversity. Antenna diversity is a technique that maximises the performance of an antenna system. It allows the radio to switch between two antennas that have very low correlation between their received signals. Typically, this is achieved by spacing two antennas around 0.25 wavelengths apart or by using two orthogonal polarisations. So, if a packet is transmitted and no acknowledgement is received, the radio system can switch to the other antenna for the retry, with a different probability of success.

The JN5139 provides an output on DIO12 that is asserted on odd numbered retries that can be used to control an antenna switch; this enables antenna diversity to be implemented easily (see Figure 16 and Figure 17)

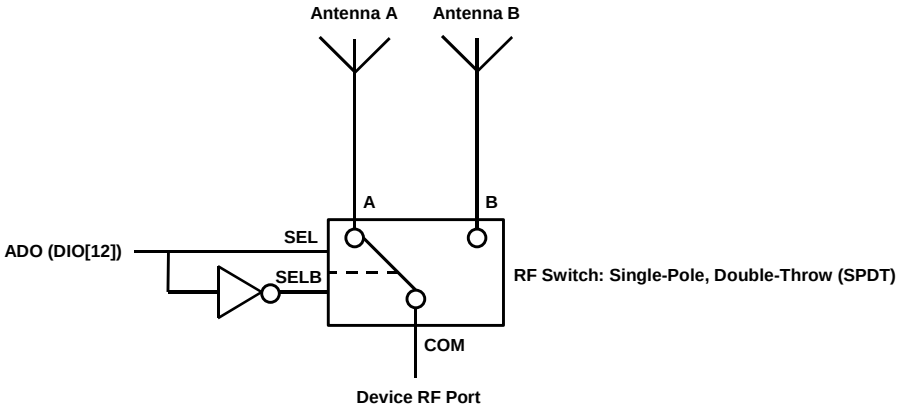


Figure 16 Simple Antenna Diversity Implementation using External RF Switch

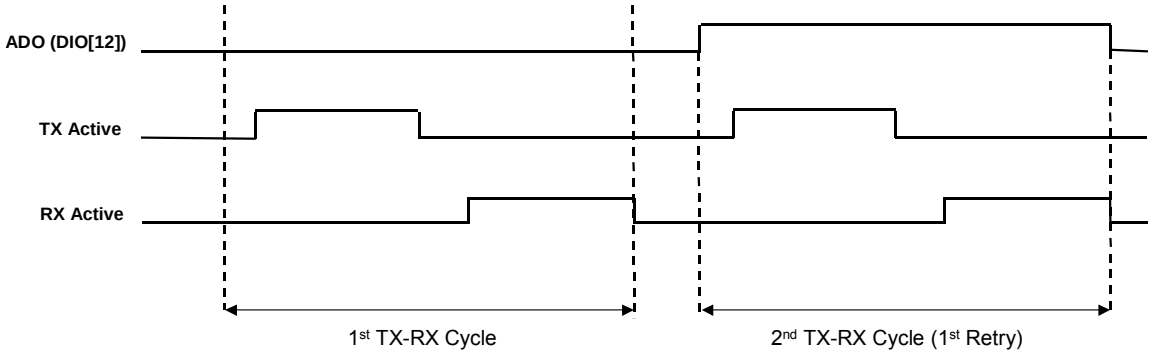


Figure 17 Antenna Diversity ADO Signal for TX with Acknowledgement

8.2 Modem

The Modem performs all the necessary modulation and spreading functions required for digital transmission and reception of data at 250kbps in the 2450MHz radio frequency band in compliance with the IEEE802.15.4 standard.

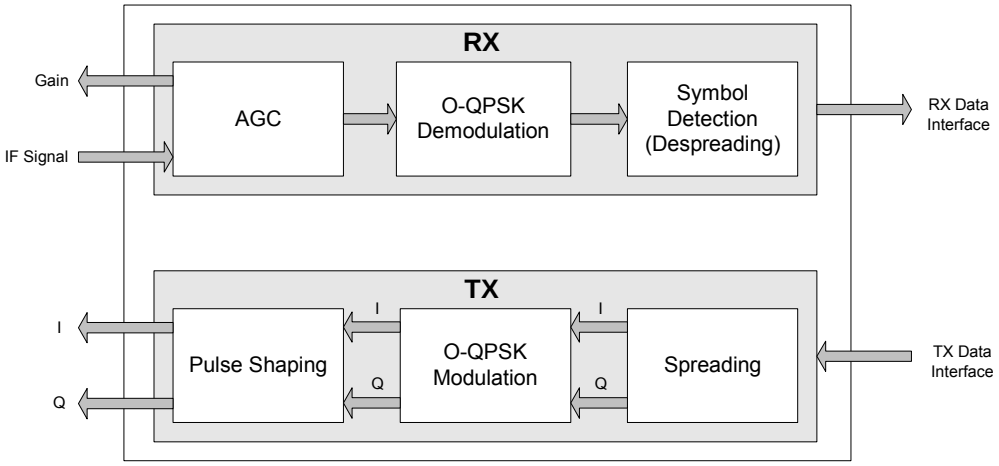


Figure 18: Modem Architecture

The transmitter receives symbols from the baseband processor and uses the spreading function to map each unique 4-bit symbol to a 32-chip Pseudo-random Noise (PN) sequence. Offset-QPSK modulation and half-sine pulse shaping is applied to the resultant spreading sequence to produce two independent quadrature phase signals (I and Q), which are subsequently converted to analogue voltages in the radio transmit path.

The Automatic Gain Control (AGC) monitors the received signal level and adjusts the gain of the amplifiers in the radio receiver to ensure that the optimum signal amplitude is maintained during reception.

The demodulator performs digital IF down-conversion and matched filtering and is extremely tolerant to carrier frequency offsets in excess of ±80ppm without suffering any significant degradation in performance.

Symbol detection and synchronization is performed using direct sequence correlation techniques in conjunction with searches for the Preamble and Start-of-Frame Delimiter (SFD) fields contained in the transmitted IEEE 802.15.4 Synchronization Header (SHR).

Features are provided to support network channel selection algorithms include Energy Detection (ED), Link Quality Indication (LQI) and fully programmable Clear Channel Assessment (CCA).

The Modem provides a digital Receive Signal Strength Indication (RSSI) that facilitates the implementation of the IEEE 802.15.4 ED function.

The LQI is defined in the IEEE 802.15.4 standard as a characterization of the strength and/or data quality of a received packet. The Modem produces a signal quality metric based upon correlation magnitudes, which may be used in conjunction with the ED value to formulate the LQI.

The CCA capability of the Modem supports all modes of operation defined in the IEEE 802.15.4 standard, namely Energy above ED threshold, Carrier Sense and Carrier Sense and/or energy above ED threshold.

8.3 Baseband Processor

The baseband processor provides all time-critical functions of the IEEE802.15.4 MAC layer. Dedicated hardware guarantees air interface timing is precise. The MAC layer hardware/software partitioning enables software to implement the sequencing of events required by the protocol and to schedule timed events with millisecond resolution, and the hardware to implement specific events with microsecond timing resolution. The protocol software layer performs the higher-layer aspects of the protocol, sending management and data messages between endpoint and coordinator nodes, using the services provided by the baseband processor.

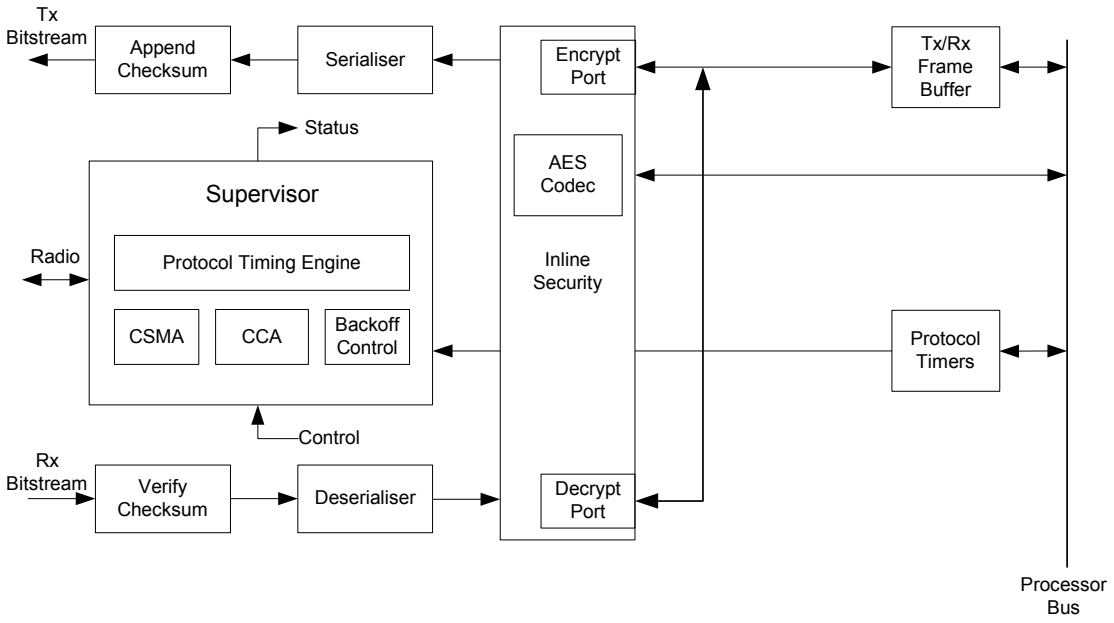


Figure 19: Baseband Processor

8.3.1 Transmit

A transmission is performed by software writing the data to be transferred into the Tx/Rx Frame Buffer, together with parameters such as the destination address and the number of retries allowed, and programming one of the protocol timers to indicate the time at which the frame is to be sent. This time will be determined by the software tracking the higher-layer aspects of the protocol such as superframe timing and slot boundaries. Once the packet is prepared and protocol timer set, the supervisor block controls the transmission. When the scheduled time arrives, the supervisor controls the sequencing of the radio and modem to perform the type of transmission required. It can perform all the algorithms required by IEEE802.15.4 such as CSMA/CA including retries and random backoffs without processor intervention.

When the transmission begins, the header of the frame is constructed from the parameters programmed by the software and sent with the frame data through the serialiser to the Modem. At the same time, the radio is prepared

for transmission. During the passage of the bitstream to the modem, it passes through a CRC checksum generator that calculates the checksum on-the-fly, and appends it to the end of the frame.

If using slotted access, it is possible for a transmission to overrun the time in its allocated slot; the Baseband Processor handles this situation autonomously and notifies the protocol software via interrupt, rather than requiring it to handle the overrun explicitly.

8.3.2 Reception

During reception, the radio is set to receive on a particular channel. On receipt of data from the modem, the frame is directed into the Tx/Rx Frame Buffer where both header and frame data can be read by the protocol software. An interrupt may be provided on receipt of the frame header. As the frame data is being received from the modem it is passed through a checksum generator; at the end of the reception the checksum result is compared with the checksum at the end of the message to ensure that the data has been received correctly. An interrupt may be provided to indicate successful packet reception.

During reception, the modem determines the Link Quality, which is made available at the end of the reception as part of the requirements of IEEE802.15.4.

8.3.3 Auto Acknowledge

Part of the protocol allows for transmitted frames to be acknowledged by the destination sending an acknowledge packet within a very short window after the transmitted frame has been received. The JN5139 baseband processor can automatically construct and send the acknowledgement packet without processor intervention and hence avoid the protocol software being involved in time-critical processing within the acknowledge sequence. The JN5139 baseband processor can also request an acknowledge for packets being transmitted and handle the reception of acknowledged packets without processor intervention.

8.3.4 Beacon Generation

In beaconing networks, the baseband processor can automatically generate and send beacon frames; the repetition rate of the beacons is programmed by the CPU, and the baseband then constructs the beacon contents from data delivered by the CPU. The baseband processor schedules the beacons and transmits them without CPU intervention.

8.3.5 Security

The baseband processor supports the transmission and reception of secured frames using the Advanced Encryption Standard (AES) algorithm transparently to the CPU. This is done by passing incoming and outgoing data through an in-line security engine that is able to perform encryption and decryption operations on-the-fly, resulting in minimal processor intervention. The CPU must provide the appropriate encrypt/decrypt keys for the transmission or reception. On transmission, the key can be programmed at the same time as the rest of the frame data and setup information.

During reception, the CPU must look up the key and provide it from information held in the header of the incoming frame. However, the hardware of the security engine can process data much faster than the incoming frame data rate. This means that it is possible to allow the CPU to receive the interrupt from the header of an incoming packet, read where the frame originated, look up the key and program it to the security hardware before the end of the frame has arrived. By providing a small amount of buffering to store incoming data while the lookup process is taking place, the security engine can catch up processing the frame so that when the frame arrives in the receive frame buffer it is fully decrypted.

8.4 Security Coprocessor

As well as being used during in-line encryption/decryption operations over a streaming interface and in external memory encryption, it is also possible to use the AES core as a coprocessor to the CPU of the JN5139. To allow the hardware to be shared between the two interfaces an arbiter ensures that the streaming interface to the AES core always has priority, to ensure that in-line processing can take place at any time.

Some protocols require that security operations can be performed on buffered data rather than in-line. A hardware implementation of the encryption engine significantly speeds up the processing of the contents of these buffers. The Security Coprocessor can be accessed through software to allow the contents of memory buffers to be transformed.

Information such as the type of security operation to be performed and the encrypt/decrypt key to be used must also be provided.

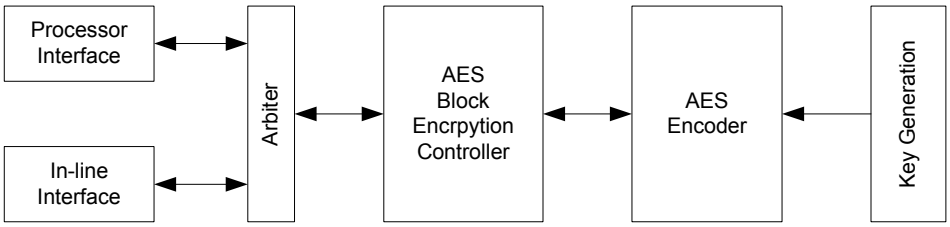


Figure 20: Security Coprocessor Architecture

9 Digital Input/Output

There are 21 Digital I/O (DIO) pins, which can be configured as either an input or an output, and each has a selectable internal pull-up resistor. Most DIO pins are multiplexed with alternate peripheral features of the device, see section 2. Once a peripheral is enabled it takes precedence over the device pins. Refer to the individual module sections for a full description of the alternate peripherals functions. Following a reset (and whilst the reset input is held low), all peripherals are off and the DIO pins are configured as inputs with the internals pull-ups turned on.

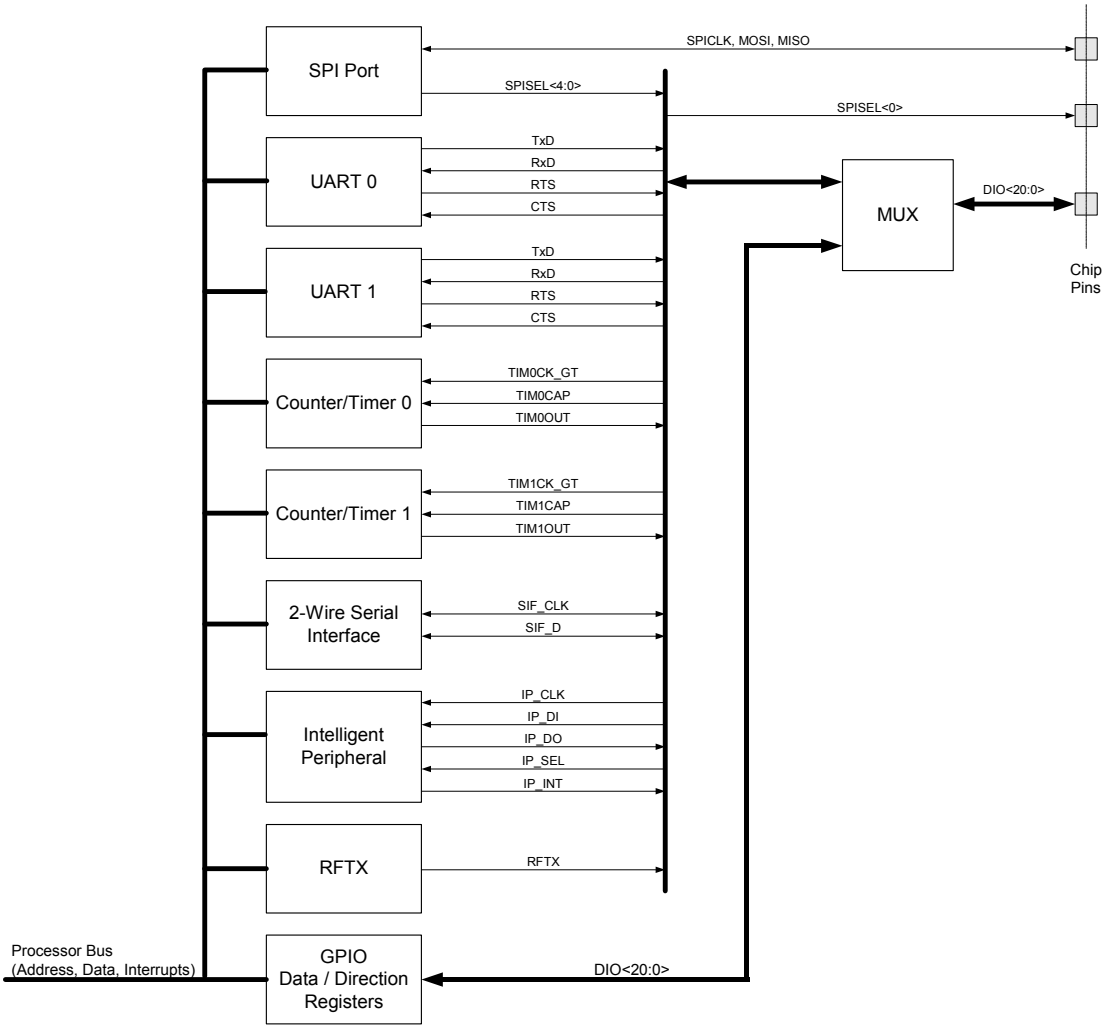


Figure 21: DIO Block Diagram

When a peripheral is not enabled, the DIO pins associated with it can be used as digital inputs or outputs. Each pin can be controlled individually by setting the direction and then reading or writing to the pin.

The individual pull-up resistors, R_{PU}, can also be enabled or disabled as needed and the setting is held through sleep cycles. The pull-ups are generally configured once after reset depending on the external components and functionality. For instance, outputs should generally have the pull-ups disabled. An input that is always driven should also have the pull-up disabled.

When configured as an input each pin can be used to generate an interrupt upon a change of state (selectable transition either from low to high or high to low); the interrupt can be enabled or disabled. When the device is sleeping, these interrupts become events that can be used to wake the device up. Equally the status of the interrupt may be read. See section 16 Power Management and Sleep Modes for further details on sleep and wakeup.

The state of all DIO pins can be read, irrespective of whether the DIO is configured as an input or an output.

Throughout a sleep cycle the direction of the DIO, and the state of the outputs, is held. This is based on the resultant of the GPIO Data/ Direction registers and the effect of any enabled peripherals at the point of entering sleep. Following a wake-up these directions and output values are maintained under control of the GPIO data / direction registers. Any peripherals enabled before the sleep cycle are not automatically re-enabled, this must be done through software after the wake-up.

For example, if DIO0 is configured to be SPISEL1 then it becomes an output. The output value is controlled by the SPI functional block. If the device then enters a sleep cycle, the DIO will remain an output and hold the value being output when entering sleep. After wake-up the DIO will still be an output with the same value but controlled from the GPIO Data/Direction registers. It can be altered with the software functions that adjust the DIO, or the application may re-configure it to be SPISEL1.

Unused DIO pins are recommended to be set as inputs with the pull-up enabled.

10 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) allows high-speed synchronous data transfer between the JN5139 and peripheral devices. The JN5139 operates as a master on the SPI bus and all other devices connected to the SPI are expected to be slave devices under the control of the JN5139 CPU. The SPI includes the following features:

- Full-duplex, three-wire synchronous data transfer
- Programmable bit rates up to 16Mbps
- Programmable transaction size of 8,16 or 32 bits
- Supports standard SPI modes 0, 1, 2, 3 to allow control over the relationship between clock and transmit / receive data
- Automatic slave select generation (up to 5 slaves)
- Maskable transaction complete interrupt
- LSB First or MSB First Data Transfer

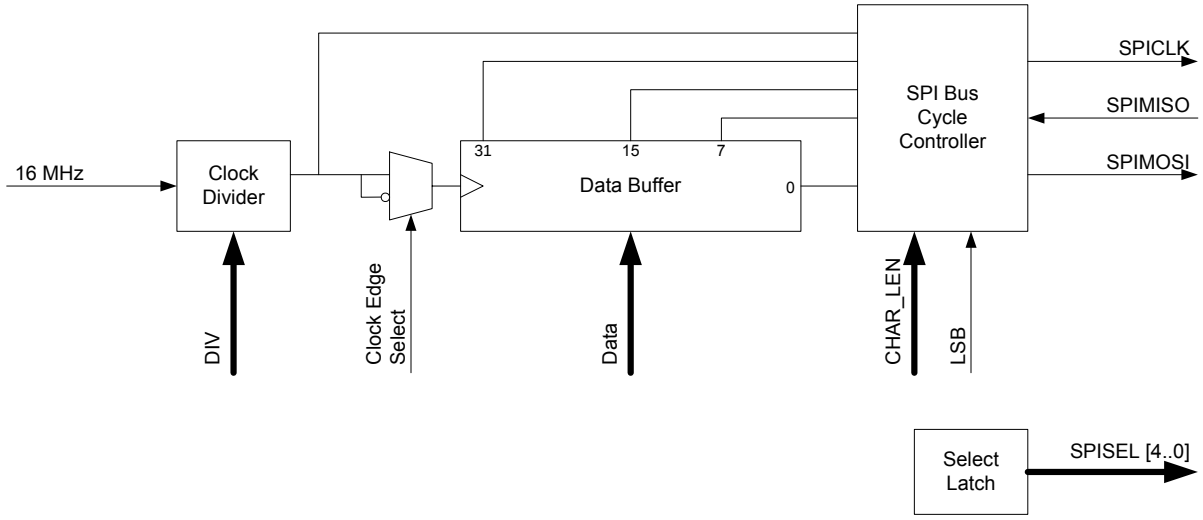


Figure 22: SPI Block Diagram

The SPI bus employs a simple shift register data transfer scheme. Data is clocked out of and into the active devices in a first-in, first-out fashion allowing SPI devices to transmit and receive data simultaneously.

There are three dedicated pins SPICLK, SPIMOSI, SPIMISO that are shared across all devices on the bus. Master-Out-Slave-In or Master-In-Slave-Out data transfer is relative to the clock signal SPICLK generated by the JN5139.

The JN5139 provides five slave selects, SPISEL0 to SPISEL4 to allow five SPI peripherals on the bus. SPISEL0 is a dedicated pin and SPISEL1 to 4, are alternate functions of pins DIO0 to 3 respectively. This allows a serial flash memory to be connected to SPISEL0 and download to internal RAM via software from reset, as part of the boot process, see section 4.4.

The interface can transfer 8, 16 or 32 bits without software intervention and can keep the slave select lines asserted between transfers when required, to enable longer transfers to be performed.

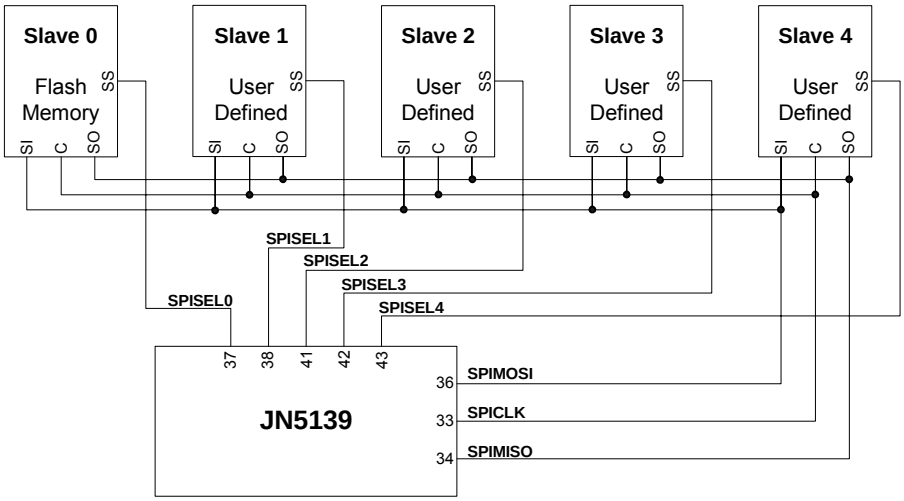


Figure 23: Typical JN5139 SPI Peripheral Connection

The data transfer rate on the SPI bus is determined by the SPICLK signal. The JN5139 supports transfers at selectable data rates from 16MHz to 250kHz selected by a clock divider. Both SPICLK clock phase and polarity are configurable. The clock polarity controls if SCLK is high or low between transfers (and hence the polarity of the first clock edge in a transfer). The clock phase and polarity determines which edge of SPICLK is used by the JN5139 to present new data on the SPIMOSI line; the opposite edge will be used to read data from the SPIMISO line. The interface should be configured appropriately for the SPI slave being accessed.

SPICLK		Mode	Description
Polarity (CPOL)	Phase (CPHA)		
0	0	0	SPICLK is low when idle – the first edge is positive. Valid data is output on SPIMOSI before the first clock and changes every negative edge. SPIMISO is sampled every positive edge.
0	1	1	SPICLK is low when idle – the first edge is positive. Valid data is output on SPIMOSI every positive edge. SPIMISO is sampled every negative edge.
1	0	2	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI before the first clock edge and is changed every positive edge. SPIMISO is sampled every negative edge.
1	1	3	SPICLK is high when idle – the first edge is negative. Valid data is output on SPIMOSI every negative edge. SPIMISO is sampled every positive edge.

Table 3 SPI Configurations

If more than one SPISEL line is to be used in a system they must be used in numerical order, for instance if 3 SPI select lines are to be used, they must be SPISEL0, 1 and 2. A SPISEL line can be configured to automatically deassert between transactions if required, or it may stay asserted over a number of transactions. For devices such as memories where a large amount of data can be received by the master by continually providing SPICLK transitions, the ability for the select line to stay asserted is an advantage since it keeps the slave enabled over the whole of the transfer.

A transaction commences with the SPI bus being set to the correct configuration, and then the slave device is selected. Upon commencement of transmission (8, 16 or 32 bits) data is placed in the FIFO data buffer and clocked out, at the same time generating the corresponding SPICLK transitions. Since the transfer is full-duplex, the same number of data bits is being received from the slave as it transmits. The data that is received during this transmission can be read 8, 16 or 32 bits. If the master simply needs to provide a number of SPICLK transitions to allow data to be sent from a slave, it should perform transmit using dummy data. An interrupt can be generated when the transaction has completed or alternatively the interface can be polled.

If a slave device wishes to signal the JN5139 indicating that it has data to provide, it may be connected to one of the DIO pins that can be enabled as an interrupt.

11 Intelligent Peripheral Interface

The Intelligent Peripheral (IP) Interface is provided for systems that are more complex, where there is a processor that requires a wireless peripheral. As an example, the JN5139 may provide a complete JenNet wireless network interface to a phone, computer, PDA, set-top box or games console. No resources are required from the main processor compared to a transceiver as the complete wireless protocol may be run on the internal JN5139 CPU. The wireless peripheral may be controlled via one of the UARTs but the IP interface is intended to provide a high-speed, low-processor-overhead interface. The IP interface cannot be used with the CPU in doze.

The intelligent peripheral interface is a SPI slave interface and uses pins shared with other DIO signals. The interface is designed to allow message passing and data transfer. Data received and transmitted on the IP interface is copied directly to and from a dedicated area of memory without intervention from the CPU. This memory area, the intelligent peripheral memory block, contains 64 32-bit word receive and transmit buffers.

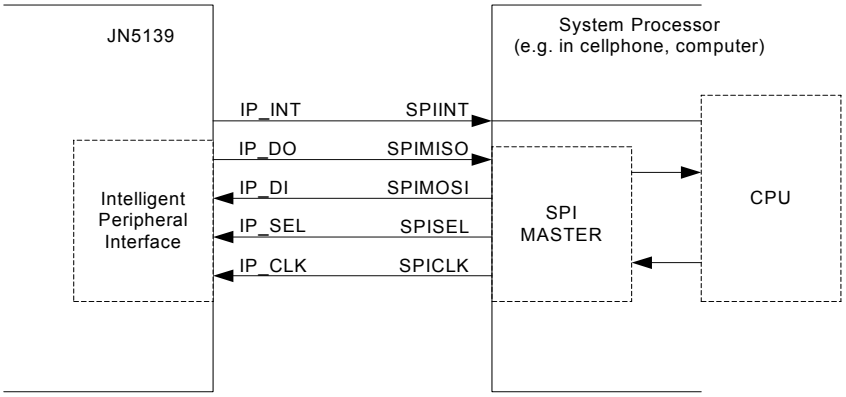


Figure 24: Intelligent Peripheral Connection

The interface functions as a SPI slave. It is possible to select the clock edge of IP_CLK on which data on the IP_DIN line of the interface is sampled, and the state of data output IP_DOUT is changed. The order of transmission is MSB first. The IP_DO data output is tri-stated when the device is inactive, i.e. the device is not selected via IP_SEL. An interrupt output line IP_INT is available so that the JN5139 can indicate to an external master that it has data to transfer. The interface can be clocked at up to 8MHz.

The IP interface signals IP_CLK, IP_DO, IP_DI, IP_SEL, IP_INT are alternate functions of pins DIO14 to 18 respectively.

11.1 Data Transfer Format

Transfers are started by the remote processor asserting the IP_SEL line and terminated by the remote processor de-asserting IP_SEL.

Data transfers are bi-directional and traffic in both directions has a format of status byte, data length byte (of the number of 32-bit words to transfer) and data packet (from the receive and transmit buffers), as shown in Figure 25. The first byte transferred into the JN5139 is a status byte with the format shown in Table 4. This is followed by a padding byte that should be set to zero. The first byte output by the JN5139 is a padding byte, that should be ignored, followed by a status byte with the format shown in Table 4

Bit	Field	Description
7:2	RSVD	Reserved, set to 0.
1	TXQ	1: Data queued for transmission
0	RXRDY	1: Buffer ready to receive data

Table 4: IP Status Byte Format

If data is queued for transmission and the recipient has indicated that they are ready for it (RXRDY in incoming status byte was 1), the next byte to be transmitted is the data length in words. If either the JN5139 or the remote processor has no data to transfer, then the data length should be set to zero. The transaction can be terminated by the master after the status and padding bytes have been sent if it is not possible to send data in either direction. This may be

because neither party has data to send or because the receiver does not have a buffer available. If the data length is non-zero, the data in the JN5139 transmit memory buffer is sent, beginning at the start of the buffer. At the same time that data bytes are being sent from the transmit buffer, the JN5139 receive buffer is being filled with incoming data, beginning from the start of the buffer.

The remote processor, acting as the master, must determine the larger of its incoming or outgoing data transfers and deassert IP_SEL when all of the transmit and receive data has been transferred. The data is transferred into or out of the buffers starting from the lowest address in the buffer, and each word is assembled with the MSB first on the serial data lines. Following a transaction, IP_SEL must be high (deasserted) for at least 300nsec before a further transaction can begin.

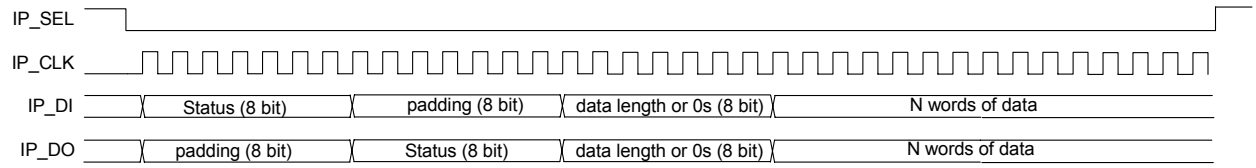


Figure 25: Intelligent Peripheral Data Transfer Waveform

11.2 JN5139 (Slave) Initiated Data Transfer

To send data, the data is written into either buffer 0 or 1 of the intelligent peripheral memory area. Then the buffer number is written together with the data length. If the call is successful, the interrupt line IP_INT will signal to the remote processor that there is a message ready to be sent from the JN5139. When a remote processor starts a transfer to the JN5139 by deasserting IP_SEL, then IP_INT is deasserted. If the transfer is unsuccessful and the data is not output then IP_INT is reasserted after the transfer to indicate that data is still waiting to be sent.

The interface can be configured to generate an internal interrupt whenever a transaction completes (for example IP_SEL becomes inactive after a transfer starts). It is also possible to mask the interrupt. The end of the transmission can be signalled by an interrupt, or the interface can be polled.

To receive data the interface must be firstly initialised and when this is done, the bit RXRDY sent in the status byte from the IP block will show that data can be received by the JN5139. Successful data arrival can be indicated by an interrupt, or the interface can be polled. IP_INT is asserted if the JN5139 is configured to be able to receive, and the remote processor has previously attempted to send data but the RXRDY indicated that it could not be sent.

To send and receive at the same time, the transmit and receive buffers must be set to be different.

11.3 Remote Processor (Master) Initiated Data Transfer

The remote processor (master) must initiate a transfer to send data to the JN5139 (slave) by asserting the slave select pin, IP_SEL, and generating its status byte on IP_DI with TXRDY set. After receiving the status byte from the JN5139, the master should check that the JN5139 has a buffer ready by reading the RXRDY bit of the received status byte. If the RXRDY bit is 0 indicating that the JN5139 cannot accept data, it must terminate the transfer by deasserting IP_SEL unless it is receiving data from the JN5139. If the RXRDY bit is 1, indicating that the JN5139 can accept data, then the master should generate a further 8 clocks on IP_CLK in order to transfer its own message length on IP_DI. The master must continue clocking the interface until sufficient clocks have been generated to send all the data specified in the length field to the JN5139. The master must then deassert IP_SEL to show the transfer is complete.

The master may initiate a transfer to read data from the JN5139 by asserting the slave select pin, IP_SEL, and generating its status byte on IP_DI with RXRDY set. After receiving the status byte from the JN5139, it should check that the JN5139 has a buffer ready by reading the TXRDY bit of the received status byte. If the TXRDY bit is 0, indicating that the JN5139 does not have data to send, it must terminate the transfer by deasserting IP_SEL unless it is transmitting data to the JN5139. If the TXRDY bit is 1, indicating that the JN5139 can send data, then the master must generate a further 8 clocks on IP_CLK in order to receive the message length on IP_DO. The master must continue clocking the interface until sufficient clocks have been generated to receive all the data specified in the length field from the JN5139. The master should then deassert IP_SEL to show the transfer is complete.

Data can be sent in both directions at once and the master must ensure both transfers have completed before deasserting IP_SEL.

Note: The remote processor must not attempt to transfer before a previous receive has been processed.

12 Timers

12.1 Peripheral Timer / Counters

Two general-purpose timer / counter units are available that can be independently configured to operate in one of five modes. The timers have the following features:

- 5-bit prescaler, divides system clock by 2 $^{\text{prescale value}}$ as the clock to the timer (prescaler range is 0 to 16)
- Clocked from internal system clock
- 16-bit counter, 16-bit Rise and Fall (period) registers
- Timer: can generate interrupts off Rise and Fall counts. Can be gated by external signal
- Counter: counts number of transitions on external event signal. Can use low-high, high-low or both transitions
- PWM/Single pulse: outputs repeating Pulse Width Modulation signal or a single pulse. Can set period and mark-space ratio
- Capture: measures times between transitions of an applied signal.
- Delta-Sigma: Return-To-Zero (RTZ) and Non-Return-to-Zero (NRZ) modes

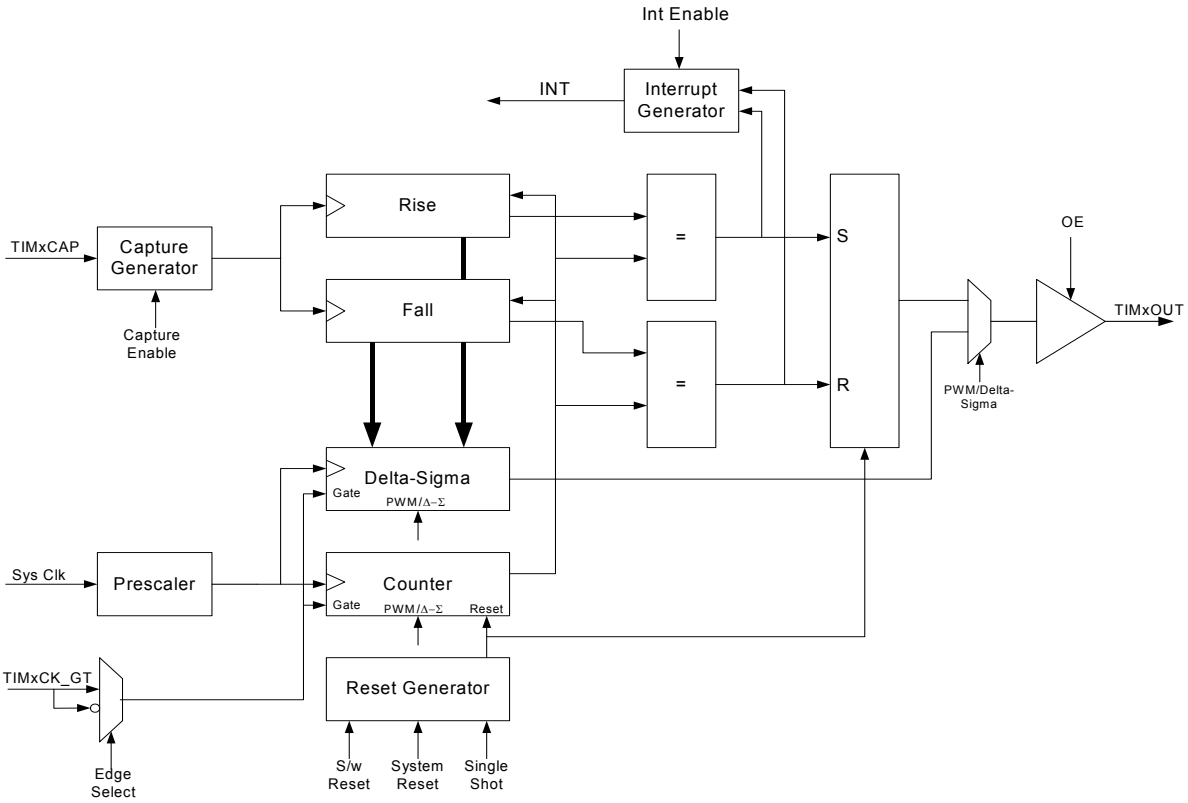


Figure 26: Timer Unit Block Diagram

The clock source for the timer unit is fed from the 16MHz system clock. This clock passes to a 16-bit prescaler where a value of 0 leaves the clock unmodified and other values divide it by 2 $^{\text{prescale}}$ value. For example, a prescale value of 2 applied to the 16MHz system clock source results in a timer clock of 4MHz. The value of the prescaler is set through software.

The counter is optionally gated by a signal on the clock / gate input (TIMxCK_GT). If the gate function is selected the counter is frozen when the clock/gate input is high.

An interrupt can be generated when the counter is equal to the value in either of the High or Low registers.

The internal Output Enable (OE) signal enables or disables the timer output.

The Timer 0 signals CK_GT, CAP and OUT are alternative functions of pins DIO8, 9 and 10 respectively and Timer 1 signals CK_GT, CAP and OUT are alternative functions of pins DIO11, 12, and 13 respectively. Selection of either the Timer or DIOx functionality is made through software, in either case the timer still functions internally.

Note, timer 0 may only be used internally when an external 32kHz clock source is used.

12.1.1 Pulse Width Modulation Mode

Pulse Width Modulation (PWM) mode allows the user to specify an overall cycle time and pulse length within the cycle. The pulse can be generated either as a single shot or as a train of pulses with a repetition rate determined by the cycle time.

In this mode, the cycletime and low periods of the PWM output signal can be set by the values of two independent 16-bit registers (Fall and Rise). The counter increments and its output is compared to the 16-bit Rise and Fall registers. When the counter is equal to the Rise register, the PWM output is set to high; when the counter reaches the Fall value, the output returns to low. In continuous mode, when the counter reaches the Fall value, it will reset and the cycle repeats. The PWM waveform is available on TIMxOUT when the output driver is enabled.

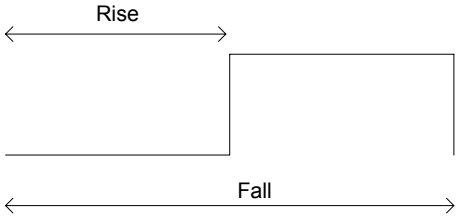


Figure 27: PWM Output Timings

12.1.2 Capture Mode

The capture mode can be used to measure the time between transitions of a signal applied to the capture input (TIMxCAP). When the capture is started, on the next low-to-high transition of the captured signal, the count value is stored in the Rise register, and on the following high-to-low transition, the counter value is stored in the Fall register. The pulse width is the difference in counts in the two registers multiplied by the period of the prescaled clock . Upon reading the capture registers the counter is stopped. The values in the High and Low registers will be updated whenever there is a corresponding transition on the capture input, and the value stored will be relative to when the mode was started. Therefore, if multiple pulses are seen on TIMxCAP before the counter is stopped only the last pulse width will be stored.

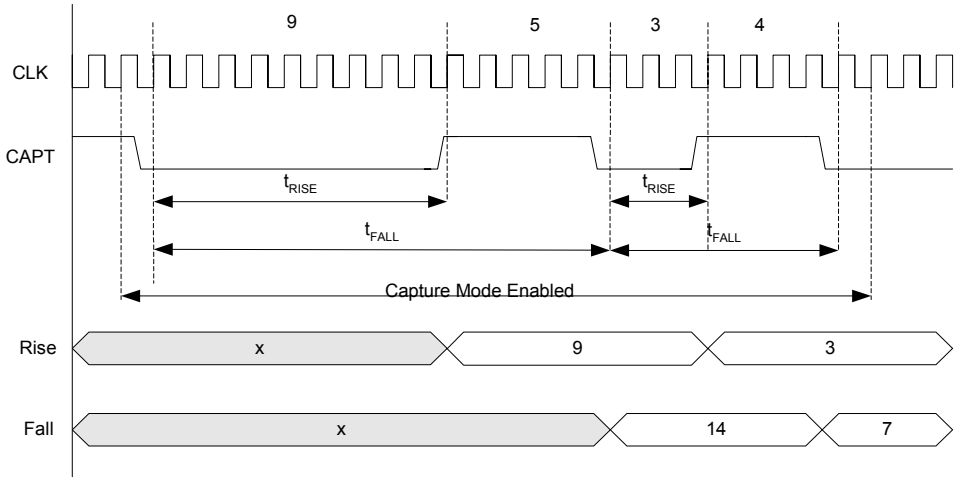


Figure 28: Capture Mode

12.1.3 Counter / Timer Mode

The counter/timer can be used to generate interrupts, based on the timers or event counting, for software to use. As a timer the clock source is from the system clock, prescaled if required. The timer period is programmed into the Fall register and the Fall register match interrupt enabled. The timer is started as either a single-shot or a repeating timer, and generates an interrupt when the counter reaches the Fall register value.

When used to count external events on TIMxCK_GT the clock source is selected from the input pin and the number of events programmed into the Fall register. The Fall register match interrupt is enabled and the counter started, usually in single shot mode. An interrupt is generated when the programmed number of transitions is seen on the input pin. The transitions counted can be configured to be rising, falling or both rising and falling edges.

Edges on the event signal must be at least 100nsec apart, i.e. pulses must be wider than 100nsec.

12.1.4 Delta-Sigma Mode

A separate delta-sigma mode is available, allowing a low speed delta-sigma DAC to be implemented with up to 16-bit resolution. This requires that a resistor-capacitor network is placed between the output DIO pin and digital ground. A stream of pulses with digital voltage levels is generated which is integrated by the RC network to give an analogue voltage. A conversion time is defined in terms of a number of clock cycles. The width of the pulses generated is the period of a clock cycle. The number of pulses output in the cycle, together with the integrator RC values will determine the resulting analogue voltage. For example, generating approximately half the number of pulses that make up a complete conversion period will produce a voltage on the RC output of VDD1/2, provided the RC time constant is chosen correctly. During a conversion, the pulses will be pseudo-randomly dispersed throughout the cycle in order to produce a steady voltage on the output of the RC network.

The output signal is asserted for the number of clock periods defined in the High register, with the total period being 2^{16} cycles. For the same value in the High register the pattern of pulses on subsequent cycles is different, due to the pseudo-random distribution.

The delta-sigma convertor output can operate in a Return-To-Zero (RTZ) or a Non-Return-to-Zero (NRZ) mode. The NRZ mode will allow several pulses to be output next to each other. The RTZ mode ensures that each pulse is separated from the next by at least one period. This improves linearity if the rise and fall times of the output are different to one another. Essentially, the output signal is low on every other output clock period, and the conversion cycle time is twice the NRZ cycle time ie 2^{17} clocks. The integrated output will only reach half VDD2 in RTZ mode, since even at full scale only half the cycle contains pulses. Figure 29 and Figure 30 illustrate the difference between RTZ and NRZ for the same programmed number of pulses.

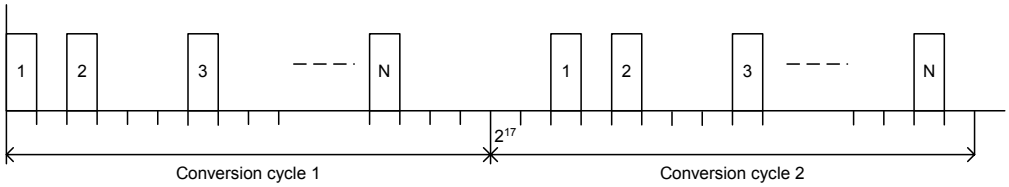


Figure 29: Return To Zero Mode in Operation

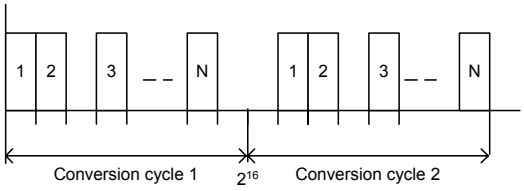


Figure 30: Non-Return to Zero Mode

12.1.5 Timer / Counter Application

Figure 31 shows an application of the JN5139 timers to provide closed loop speed control. Timer 0 is configured in PWM mode to provide a variable mark-space ratio switching waveform to the gate of the NFET. This in turn controls the power in the DC motor.

Timer 1 is configured to count the rising edge events on the clk/gate pin over a constant period. This converts the tacho pulse stream output into a count proportional to the motor speed. This value is then used by the application software executing the control algorithm.

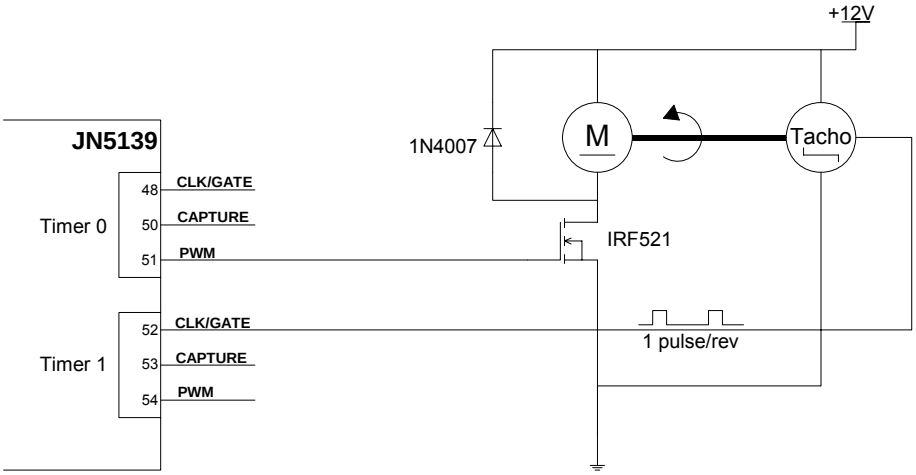


Figure 31: Closed Loop PWM Speed Control Using JN5139 Timers

12.2 Tick Timer

The JN5139 contains a hardware timer that can be used for generating timing interrupts to software. It may be used to implement regular events such as ticks for software timers or an operating system, as a high-precision timing reference or can be used to implement system monitor timeouts as used in a watchdog timer. Features include:

- 32-bit counter
- 28-bit match value
- Maskable timer interrupt
- Single-shot, Restartable or Continuous modes of operation

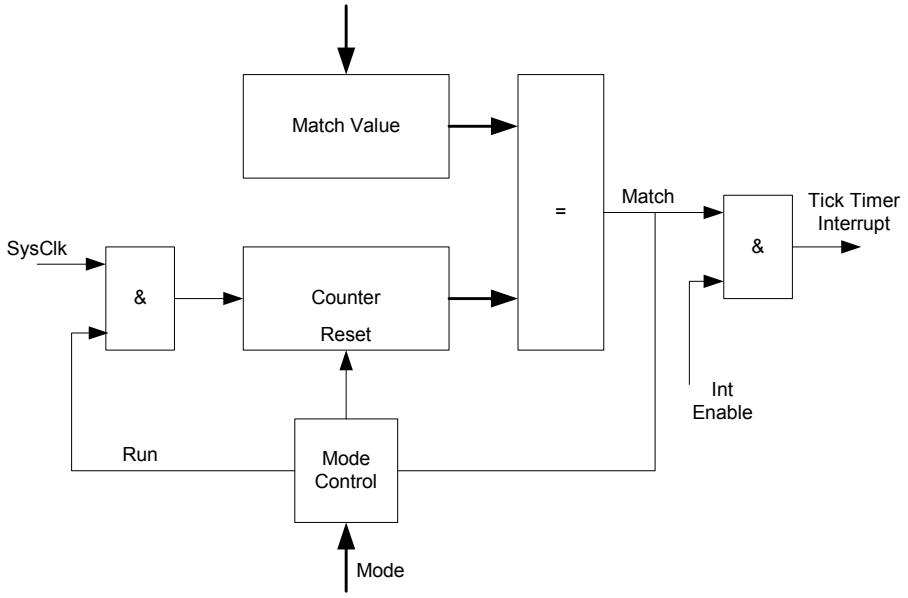


Figure 32: Tick Timer

The Tick Timer is clocked from the 16MHz CPU clock, which is fed to a 32-bit wide resettable up-counter, gated by a signal from the mode control block. A match register allows comparison between the counter and a programmed value. The match value, measured in 16MHz clock cycles is programmed through software, in the range 0 to 0x0FFFFFFF. The output of the comparison can be used to generate an interrupt if the interrupt is enabled and used in controlling the counter in the different modes. Upon configuring the timer mode, the counter is also reset.

If the mode is programmed as single shot, the counter begins to count from zero until the match value is reached. The match signal will be generated which will cause an interrupt if enabled, and the counter will stop counting. The counter is restarted by reprogramming the mode.

If the mode is programmed as restartable, the operation of the counter is the same as for the single shot mode, except that when the match value is reached the counter is reset and begins counting from zero. An interrupt will be generated when the match value is reached if it is enabled.

Continuous mode operation is similar to restartable, except that when the match value is reached, the counter is not reset but continues to count. An interrupt will be generated when the match value is reached if enabled.

In CPU doze mode the tick timer is not clocked and therefore cannot be used as a wakeup source.

12.3 Wakeup Timers

Two 32-bit wakeup timers driven from the 32kHz system clock are available in the JN5139. They may run during sleep periods when the majority of the rest of the device is powered down, to time sleep periods or other long period timings that may be required by the application. The wakeup timers do not run during deep sleep and may optionally be disabled in sleep mode through software control. When a wakeup timer expires it typically generates an interrupt,

if the device is asleep then the interrupt may be used as an event to end the sleep period. See Section 16 for further details on how they are used during sleep periods. Features include:

- 32-bit down-counter
- Optionally runs during sleep periods
- Clocked from either:
    - 32kHz RC Oscillator
    - 32kHz External Clock

A wakeup timer consists of a 32-bit down counter clocked from the 32 kHz system clock. An interrupt or wakeup event can be generated when the counter reaches zero. On reaching zero the counter will continue to count down until stopped, which allows the latency in responding to the interrupt to be measured. If an interrupt or wakeup event is required, the timer interrupt should be enabled before loading the count value for the period. Once the count value is loaded and counter started, the counter begins to count down; the counter can be stopped at any time through software control. The counter will remain at the value it contained when the timer was stopped and no interrupt will be generated. The status of the timers can be read to indicate if the timers are running and/or have expired; this is useful when the timer interrupts are masked. This operation will reset any expired status flags.

12.3.1 RC Oscillator Calibration

The RC oscillator that can be used to time sleep periods is designed to require very little power to operate and be self-contained, requiring no external timing components and hence is lower cost. As a consequence of using on-chip resistors and capacitors, the inherent absolute accuracy and temperature coefficient is lower than that of a crystal oscillator, but once calibrated the accuracy approaches that of a crystal oscillator. Sleep time periods should be as close to the desired time as possible in order to allow the device to wake up in time for important events, for example beacon transmissions in the IEEE802.15.4 protocol. If the sleep time is accurate, the device can be programmed to wake up very close to the calculated time of the event and so keep current consumption to a minimum. If the sleep time is less accurate, it will be necessary to wake up earlier in order to be certain the event will be captured. If the device wakes earlier, it will be awake for longer and so reduce battery life.

In order to allow sleep time periods to be as close to the desired length as possible, the true frequency of the RC oscillator needs to be determined to better than the initial 30% accuracy. The calibration factor can then be used to calculate the true number of nominal 32kHz periods needed to make up a particular sleep time. A calibration reference timer, clocked from the crystal oscillator, is provided to allow comparisons to be made between the RC clock and the 16MHz crystal oscillator when the JN5139 is awake. Operation is as follows:

- Wakeup timer0 is disabled and programmed with a number of 32kHz ticks
- Timer0 event status must be cleared
- Calibration mode is enabled which causes the Calibration Reference counter to be zeroed. Both counters start counting, the wakeup timer decrementing and the calibration counter incrementing
- When the wakeup timer reaches zero the Reference Counter is stopped, allowing software to read the number of 16MHz clock ticks generated during the time represented by the number of 32kHz ticks programmed in the wakeup timer. The true period of the 32kHz clock can thus be determined and used when programming a wakeup timer to achieve a better accuracy and hence more accurate sleep periods

For a RC oscillator running at exactly 32kHz the value returned by the calibration procedure should be 10000, for a calibration period of twenty 32kHz clock periods. If the oscillator is running faster than 32kHz the count will be less than 10000, if running slower the value will be higher. For a calibration count of 9000, indicating that the RC oscillator period is running at approximately 35kHz, to time for a period of 2 seconds the timer should be loaded with 71,111 ((10000/9000) x (32000 x 2)) rather than 64000.

13 Serial Communications

The JN5139 has two independent Universal Asynchronous Receiver / Transmitter (UART) serial communication interfaces. These provide similar operating features to the industry standard 16550A device operating in FIFO mode. Each interface performs serial-to-parallel conversion on incoming serial data and parallel-to-serial conversion on outgoing data from the CPU to external devices. In both directions, a 16-byte deep FIFO buffer allows the CPU to read and write multiple characters on each transaction. This means that the CPU is freed from handling data on a character-by-character basis, with the associated high processor overhead. The UARTs have the following features:

- Emulates behaviour of industry standard NS16450 and NS16550A UARTs
- 16 byte transmit and receive FIFO buffers reduce interrupts to CPU, with direct access to fill levels of each
- Adds / deletes standard start, stop and parity communication bits to or from the serial data
- Independently controlled transmit, receive, status and data sent interrupts
- Optional modem flow control signals CTS and RTS
- Fully programmable data formats: baud rate, start, stop and parity settings
- False start bit detection, parity, framing and FIFO overrun error detect and break indication
- Internal diagnostic capabilities: loop-back controls for communications link fault isolation
- Flow control by software or automatically by hardware

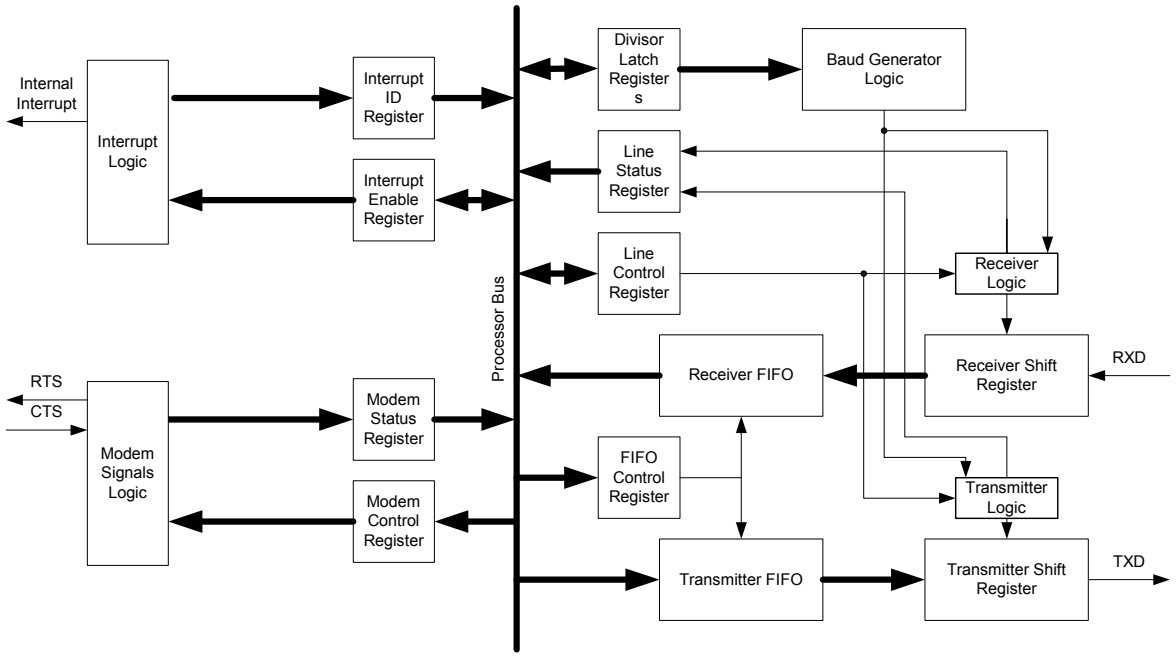


Figure 33 UART Block Diagram

The serial interface contains programmable fields that can be used to set number of data bits (5, 6,7 or 8), even, odd, set-at-1, set-at-0 or no-parity detection and generation of single or multiple stop bit, (for 5 bit data, multiple is 1.5 stop bits; for 6, 7 or 8 data bits, multiple is 2 bits).

The baud rate is programmable up to 1Mbps, standard baud rates such as 4800, 9600, 19.2k, 38.4k etc. can be configured.

Two hardware flow control signals are provided: Clear-To-Send (CTS) and Request-To-Send (RTS). CTS is an indication sent by an external device to the UART that it is ready to receive data. RTS is an indication sent by the UART to the external device that it is ready to receive data. RTS is controlled from software, while the value of CTS can be read. Monitoring and control of CTS and RTS is a software activity, normally performed as part of interrupt processing. The signals do not control parts of the UART hardware, but simply indicate to software the state of the UART external interface. Alternatively, the Automatic Flow Control mode can be set where the hardware controls the

value of the generated RTS (negated if the receive FIFO fill level is 15 and another character starts to be received, and asserted when the receive FIFO is read), and only transmits data when the incoming CTS is asserted.

Software can read characters, one byte at a time, from the Receive FIFO and can also write to the Transmit FIFO, one byte at a time. The Transmit and Receive FIFOs can be cleared and reset independently of each other. The status of the transmitter can be checked to see if it is empty, and if there is a character being transmitted. The status of the receiver can also be checked, indicating if conditions such as parity error, framing error or break indication have occurred. It also shows if an overrun error occurred (receive buffer full and another character arrives) and if there is data held in the receive FIFO.

UART 0 signals CTS, RTS, TXD and RXD are alternate functions of pins DIO4, 5, 6 and 7 respectively and UART 1 signals CTS, RTS, TXD and RXD are alternate functions of pins DIO17, 18, 19 and 20 respectively. If CTS and RTS are not required on the devices external pins, then they may be disabled. This allows the freed DIOs to be used for other purposes.

Note: The automatic hardware flow control within the UART block negates RTS when the receive FIFO is about to become full. This occurs when the UART has started receiving the last byte that it can accept. In some instances it has been observed that remote devices that are transmitting data do not respond quickly enough to the de-asserted RTS output and continue to transmit data. In these instances the data will be lost in a receive FIFO overflow, e.g. a FTDI USB to serial cable.

13.1 Interrupts

Interrupt generation can be controlled for the UART block, and is divided into four categories:

- Received Data Available: Is set when data in the Rx FIFO queue reaches a particular level (the trigger level can be configured as 1, 4, 8 or 14) or if no character has been received for 4 character times.
- Transmit FIFO Empty: set when the last character from the Tx FIFO is read and starts to be transmitted.
- Receiver Line Status: set when one of the following occur (1) Parity Error - the character at the head of the receive FIFO has been received with a parity error, (2) Overrun Error - the Rx FIFO is full and another character has been received at the Receiver shift register, (3) Framing Error - the character at the head of the receive FIFO does not have a valid stop bit and (4) Break Interrupt – occurs when the RxD line has been held low for an entire character.
- Modem Status: Generated when the CTS (Clear To Send) input control line changes.

13.2 UART Application

The following example shows the UART connected to a 9-pin connector compatible with a PC. The software developer kit uses such an interface as the debugger interface between the JN5139 and a PC. As the JN5139 device pins do not provide the RS232 line voltage a level shifter is used.

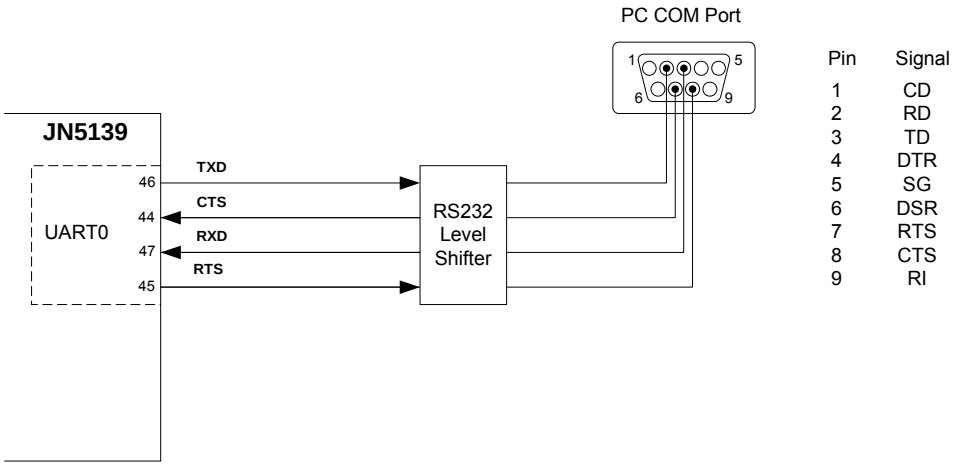


Figure 34 JN5139 Serial Communication Link

14 Two-Wire Serial interface

The JN5139 includes an industry standard two-wire synchronous serial interface (SIF) that provides a simple and efficient method of data exchange between devices. The system operates as a master only and uses a serial data line (SIF_D) and a serial clock line (SIF_CLK) to perform bi-directional data transfers; includes the following features:

- Compatible with both I^2C and SMbus peripherals (master only mode)
- Software programmable clock frequency
- Clock stretching and wait state generation
- Software programmable acknowledge bit
- Interrupt or bit-polling driven byte-by-byte data-transfers
- Bus busy detection
- Support for 7 and 10 bit addressing modes

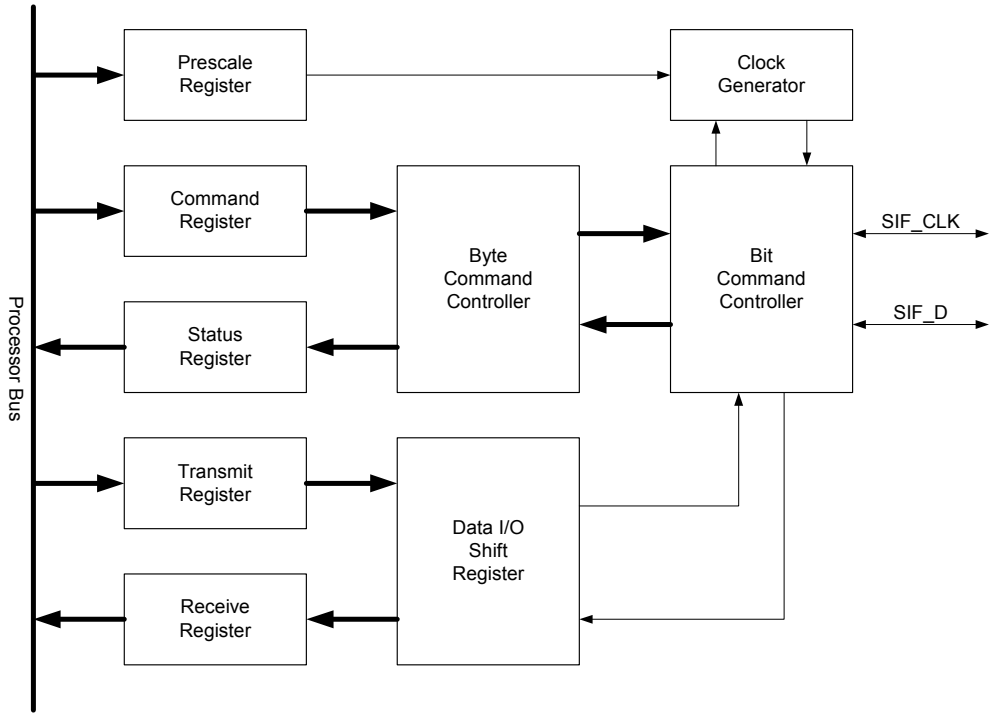


Figure 35: SIF Block Diagram

The software libraries allow full control of the underlying registers and give access to the following features.

A configurable prescale register allows the interface to be configured to operate at up to 400kbit/s. The clock generator handles the clock stretching required by some slave devices.

The Byte Command Controller handles traffic at the byte level. It takes data from the Command Register and translates it into sequences based on the transmission of a single byte. By setting the start, stop, read, write and acknowledge control bits in the command register it is possible to generate read or write sequences on the bus.

The data I/O shift register contains the data associated with the current transfer. During a read operation, data is shifted into this register from the SIF_D line. When the read is complete the byte is copied into the receive register and can be accessed.

During a write operation the contents of the transmit register are copied into the shift register and then onto the SIF_D line. It is possible to generate an interrupt upon the completion of a byte transmission or reception. If interrupt-driven communication is not desired it is possible to poll the status of the interface.

The first byte of data transferred by the device after a start bit is the slave address. The JN5139 supports both 7-bit and 10-bit slave addresses by generating either one or two address transfers. Only the slave with a matching address will respond by returning an acknowledge bit.

14.1 Connecting Devices

The clock and data lines, SIF_D and SIF_CLK, are alternative functions of DIO lines 15 and 14 respectively. The serial interface function of these pins is selected when the interface is enabled. They are both bi-directional lines, connected internally to the positive supply voltage via weak (45kΩ) programmable pull-up resistors. However, it is recommended that external 4.7kΩ pull-ups be used for reliable operation at high bus speeds, as shown in Figure 36. When the bus is free, both lines are HIGH. The output stages of devices connected to the bus must have an open-drain or open-collector in order to perform the wired-AND function. The number of devices connected to the bus is solely dependent on the bus capacitance limit of 400pF.

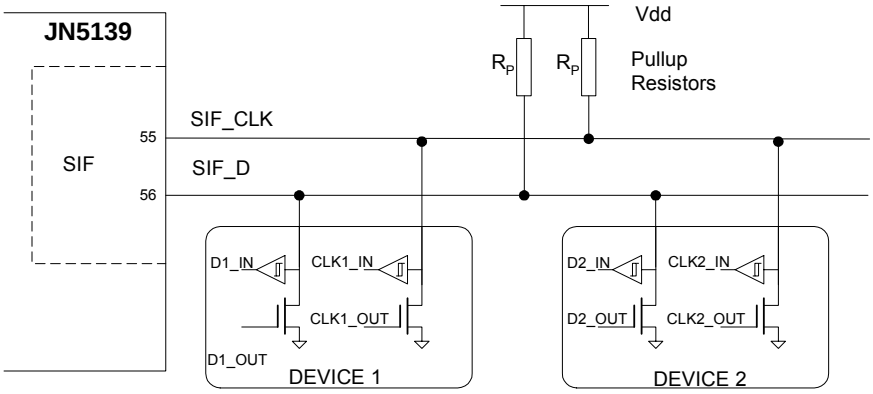


Figure 36 Connection Details

14.2 Clock Stretching

Slave devices can use clock stretching to slow down the transfer bit rate. After the master has driven SIF_CLK low, the slave can drive SIF_CLK low for the required period and then release it. If the slave's SIF_CLK low period is greater than the master's low period, the resulting SIF_CLK bus signal low period is stretched thus inserting wait states.

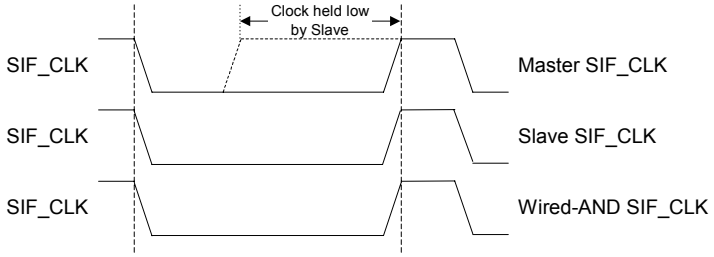


Figure 37 Clock Stretching

15 Analogue Peripherals

The JN5139 contains a number of analogue peripherals allowing the direct connection of a wide range of external sensors, switches and actuators.

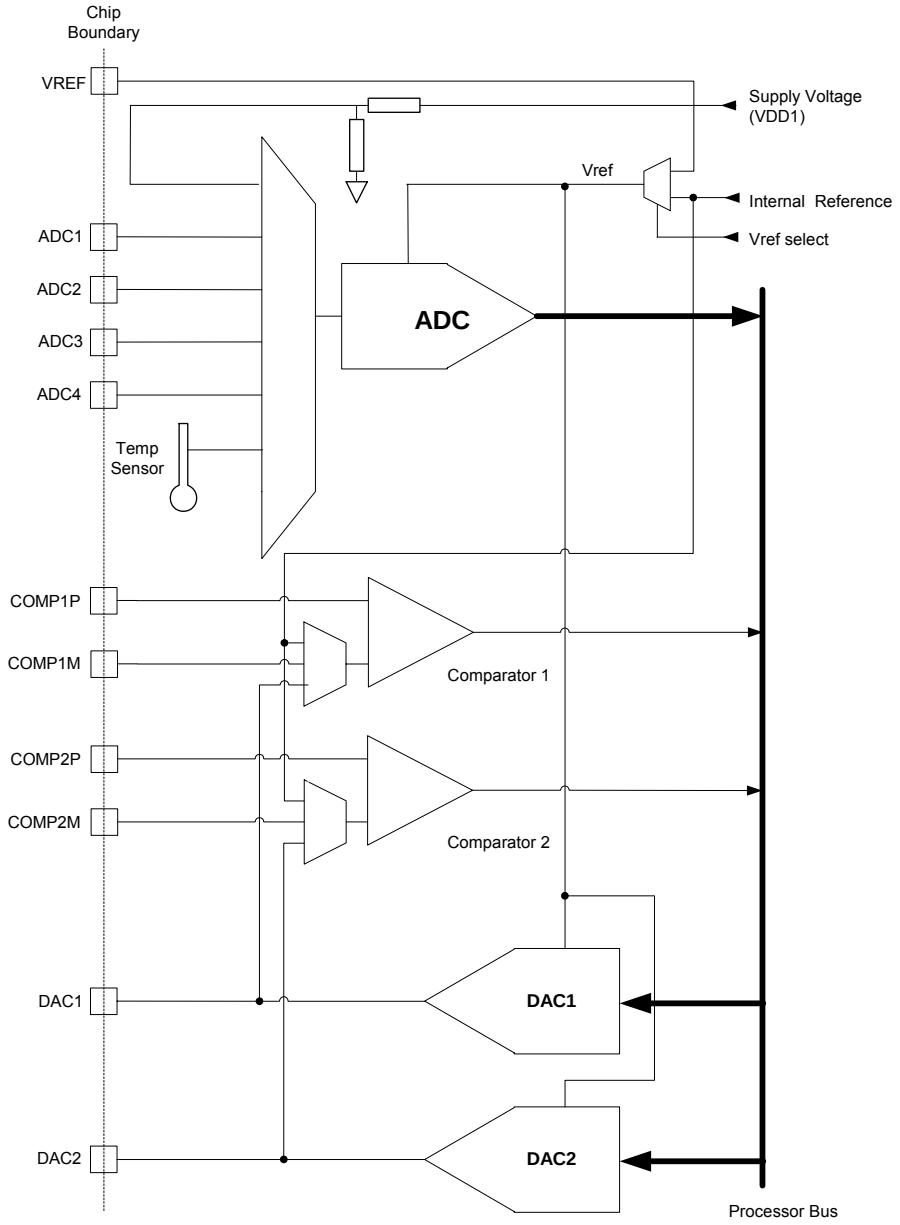


Figure 38: On-chip Analogue Peripherals

In order to provide good isolation from digital noise, the analogue peripherals are powered by a separate regulator, supplied from the analogue supply VDD1 and referenced to analogue ground VSSA.

A common reference Vref for the ADC and DAC can be selected between an internal bandgap reference or an external voltage reference supplied to the VREF pin. Gain settings for the ADC and DAC are independent of each other.

The ADC and DAC are clocked from a common clock source derived from the 16MHz clock.

15.1 Analogue to Digital Converter

The 12-bit analogue to digital converter (ADC) uses a successive approximation design to perform high accuracy conversions as typically required in wireless sensor network applications. It has six multiplexed single-ended input channels: four available externally, one connected to an internal temperature sensor, and one connected to an internal supply monitoring circuit.

15.1.1 Operation

The input range of the ADC can be set between 0V to either the reference voltage or twice the reference voltage. The reference can be either taken from the internal voltage reference or from the external voltage applied to the VREF pin. For example, an external reference of 1.2V supplied to VREF may be used to set the ADC range between 0V and 2.4V.

VREF	Gain Setting	Maximum Input Range	Supply Voltage Range (VDD)
1.2V	0	1.2V	2.2V - 3.6V
1.6V	0	1.6V	2.2V - 3.6V
1.2V	1	2.4V	2.6V - 3.6V
1.6V	1	3.2V	3.4V - 3.6V

Table 5 ADC Reference and Gain Settings

The input clock to the ADC is 16MHz and can be divided down to 2MHz, 1MHz, 500kHz and 250kHz. During an ADC conversion the selected input channel is sampled for a fixed period and then held. This sampling period is defined as a number of ADC clock periods and can be programmed to 2, 4, 6 or 8. The conversion rate is ((3 x Sample period) + 14) clock periods. For example for 500KHz conversion with sample period of 2 will be (3 x 2) + 14 = 20 clock periods, 40usecs or 25KHz. . The ADC can be operated in either a single conversion mode or alternatively a new conversion can be started as soon as the previous one has completed, to give continuous conversions.

If the source resistance of the input voltage is 1kΩ or less, then the default sampling time of 2 clocks should be used. The input to the ADC can be modelled as a resistor of 5kΩ(typ) and 10kΩ(max) to represent the on-resistance of the switches and the sampling capacitor 8pF. The sampling time required can then be calculated, by adding the sensor source resistance to the switch resistance, multiplying by the capacitance giving a time constant. Assuming normal exponential RC charging, the number of time constants required to give an acceptable error can be calculated, 7 time constants gives an error of 0.1%, so for 12-bit accuracy 10 time constants should be the target. For a source with zero resistance, 10 time constants is 800 nsecs, hence the smallest sampling window of 2 clock periods can be used.

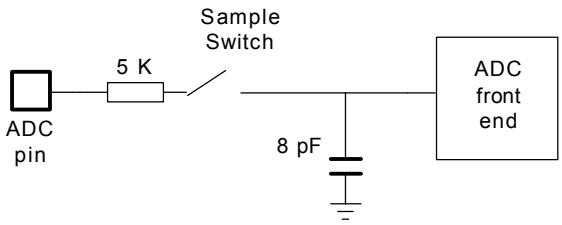


Figure 39 ADC Input Equivalent Circuit

The ADC sampling period, input range and mode (single shot or continuous) are controlled through software.

When the ADC conversion is complete, an interrupt is generated. Alternatively the conversion status can be polled. When operating in continuous mode, it is recommended that the interrupt is used to signal the end of a conversion, since conversion times may range from 10 to 152 μsecs. Polling over this period would be wasteful of processor bandwidth.

To facilitate averaging of the ADC values, which is a common practice in microcontrollers, a dedicated accumulator has been added, the user can define the accumulation to occur over 2,4,8 or 16 samples. The end of conversion interrupt can be modified to occur at the end of the chosen accumulation period, alternatively polling can still be used. Software can then be used to apply the appropriate rounding and shifting to generate the average value, as well as setting up the accumulation function.

For detailed electrical specifications, see section 17.3.9.

15.1.2 Supply Monitor

The internal supply monitor allows the voltage on the analogue supply pin VDD1 to be measured. This is achieved with a potential divider that reduces the voltage by a factor of 0.666, allowing it to fall inside the input range of the ADC when set with an input range twice the internal voltage reference. The resistor chain that performs the voltage reduction is disabled until the measurement is made to avoid a continuous drain on the supply.

15.1.3 Temperature Sensor

The on-chip temperature sensor can be used either to provide an absolute measure of the device temperature or to detect changes in the ambient temperature. In common with most on-chip temperature sensors, it is not trimmed and so the absolute accuracy variation is large; the user may wish to calibrate the sensor prior to use. The sensor forces a constant current through a forward biased diode to provide a voltage output proportional to the chip die temperature which can then be measured using the ADC. The measured voltage has a linear relationship to temperature as described in section 17.3.12.

Because this sensor is on-chip, any measurements taken must account for the thermal time constants. For example if the device recently came out of sleep mode the user application should wait until the temperature has stabilized before taking a measurement.

15.2 Digital to Analogue Converter

The Digital to Analogue Converter (DAC) provides two output channels and is capable of producing voltages of 0 to Vref or 0 to 2Vref where Vref is selected between the internal reference and the VREF pin, with a resolution of 11 bits and a minimum conversion time of 10μsecs (2MHz clock).

15.2.1 Operation

The output range of each DAC can be set independently to swing between 0V to either the reference voltage or twice the reference voltage. The reference voltage is selected from the internal reference or the VREF pin. For example, an external reference of 0.8V supplied to VREF may be used to set DAC1 maximum output of 0.8V and DAC2 maximum output of 1.6V.

The DAC output amplifier is capable of driving a capacitive load up to that specified in section 17.3.10.

Programmable clock periods allow a trade-off between conversion speed and resolution. The full 11-bit resolution is achieved with the 250kHz clock rate. See section 17.3.9, electrical characteristics, for more details.

The conversion period of the DACs are given by the same formula as the ADC conversion time and so can vary between 10 and 152uS. The DAC values may be updated at the same time as the ADC is active.

The clock divider ratio, interrupt enable and reference voltage select are all controlled through software, options common to both the ADC and DAC. The DAC output range and initial value can be set and the subsequent updates provided by updating only the DAC value. Polling is available to determine if a DAC channel is busy performing a conversion. The DAC can be disabled which will power down the DAC cell.

Simultaneous conversions with DAC1 and DAC2 is not possible. To use both DACs at the same time it is necessary to interleave the conversions. This is achieved by firstly setting the DAC1 and DAC2 retain bits, which holds the DAC outputs stable for a short time. Conversion on either channel can then be performed by disabling the unused channel and enabling the channel to be updated.

The DACs should not be used in single shot mode, but continuous conversion mode only, in order to maintain a steady output voltage.

15.3 Comparators

The JN5139 contains two analogue comparators COMP1 and COMP2 that are designed to have true rail-to-rail inputs and operate over the full voltage range of the analogue supply VDD1. The hysteresis level (common to both comparators) can be set to a nominal value of 0mV, 10mV, 20mV or 40mV. In addition, the source of the negative input signal for each comparator (COMP1M and COMP2M) can be set to the internal voltage reference, the output of DAC1 or DAC2 (COMP1 or COMP2 respectively) or the appropriate external pin. The comparator outputs are routed to internal registers and can be polled, or can be used to generate interrupts. The comparators can be disabled to reduce power consumption.

The comparators have a low power mode where the response time of the comparator is slower than normal and is specified in section 17.3.11. This mode may be used during non-sleep operation however it is particularly useful in sleep mode to wake up the JN5139 from sleep where low current consumption is important. The wakeup action and the configuration for which edge of the comparator output will be active are controlled through software. In sleep mode the negative input signal source, must be configured to be driven from the external pins.

16 Power Management and Sleep Modes

16.1 Operating Modes

Three operating modes are provided in the JN5139 that enable the system power consumption to be controlled to maximise battery life.

- Active Processing
- Sleep Mode
- Deep Sleep Mode

The variation in power consumption of the three modes is a result of having a series of power domains within the chip that may be selectably powered on or off.

16.1.1 Power Domains

The JN5139 has the following power domains:

- VDD Supply Domain: supplies the wake-up timers and controller, DIO blocks, Comparators and 32kHz RC oscillator. This domain is driven from the external supply (battery) and is always powered. The wake-up timers and controller, and the 32kHz RC oscillator may be powered on or off in sleep mode through software control.
- Digital Logic Domain: supplies the digital peripherals, CPU, ROM, Baseband controller, Modem and Encryption processor. It is powered off during sleep mode.
- Analogue Domain: supplies the ADC, DACs and the temperature sensor. It is powered off during sleep mode and may be powered on or off in active processing mode through software control.
- RAM Domain: supplies the RAM during sleep mode to retain the memory contents. It may be powered on or off for sleep mode through software control.
- Radio Domain: supplies the radio interface. It is powered during transmit and receive and controlled by the baseband processor. It is powered off during sleep mode.

The current consumption figures for the different modes of operation of the device is given in section 17.2.2.

16.2 Active Processing Mode

Active processing mode in the JN5139 is where all of the application processing takes place. All of the peripherals are available to the application as are options to actively enable or disable them to control power consumption; see specific peripheral sections for details.

To further reduce power consumption, there is also the option to doze the CPU but keep the rest of the chip active; this is particularly useful for radio transmit and receive operations, where the CPU operation is not required.

Whilst in Active processing mode there is the option to doze the CPU but keep the rest of the chip active; this is particularly useful for radio transmit and receive operations, where the CPU operation is not required.

Whilst in Active processing mode the power consumption will vary based upon whether code is being executed out of RAM or out of ROM, as the current consumption of RAM is lower than that of the ROM, so the calculation for determining the typical current is made as follows.

2.85mA + (RAM_FRACTION * 0.295mA/MHz) + (ROM_FRACTION * 0.958mA/MHz)

where RAM_FRACTION + ROM_FRACTION =1. For example, with 80% code execution from the RAM and 20% code execution from the ROM and CPU at 16MHz, the current is 9.7mA. See section 17.2.2.1 for further information on active processing current consumption.

16.2.1 CPU Doze

Whilst in doze mode, CPU operation is stopped but the chip remains powered and the digital peripherals continue to run. Doze mode is entered through software and is terminated by any interrupt request. Once the interrupt service routine has been executed, normal program execution resumes. Doze mode uses more power than sleep and deep sleep modes but requires less time to restart and can therefore be used as a low power alternative to an idle loop.

Whilst in CPU doze the current associated with the CPU drops, the RAM_FRACTION and ROM_FRACTION are both 0 and hence the base device current consumption drops to 2.85mA.

16.3 Sleep Mode

The JN5139 enters sleep mode through software control. In this mode most of the internal chip functions are shutdown to save power, however the state of DIO pins are retained, including the output values and pull-up enables, and this therefore preserves any interface to the outside world. The DAC outputs are placed into a high impedance state.

When entering into sleep mode, there is an option to retain the RAM contents throughout the sleep period. If the wakeup timers are not to be used for a wakeup event and the application does not require them to run continually, then power can be saved by switching off the 32kHz oscillator if selected as the system clock through software control. The oscillator will be restarted when a wakeup event occurs.

Whilst in sleep mode one of three possible events can cause a wakeup to occur: transitions on DIO inputs, expiry of wakeup timers or comparator events. If any of these events occur, and the relevant interrupt is enabled, then an interrupt is generated that will cause a wakeup from sleep. It is possible for multiple wakeup sources to trigger an event at the same instant and only one of them will be accountable for the wakeup period. It is therefore necessary in software to remove all other pending wakeup events prior to requesting entry back into sleep mode; otherwise, the device will re-awaken immediately.

When wakeup occurs, a similar sequence of events to the reset process described in section 6.1 happens. The 16MHz oscillator is started up, once stable the CPU system is enabled and the reset is removed. Software determines that this is a reset from sleep and so commences with the wakeup process. If the RAM contents were held through sleep, wakeup is quicker as the application program does not have to be reloaded from Flash memory. See section 17.3.5 for wake up timings.

16.3.1 Wakeup Timer Event

The JN5139 contains two 32-bit wakeup timers that are counters clocked by the 32kHz system clock, and can be programmed to generate a wake-up event. Following a wakeup event, the timers continue to run. These timers are described in section 12.3.

Timer events can be generated from both of the two timers; one is intended for use by the 802.15.4 protocol, the other being available for use by the Application running on the CPU. These timers are available to run at any time, even during sleep mode.

16.3.2 DIO Event

Any DIO pin when used as an input has the capability, by detecting a transition, to generate a wake-up event. Once this feature has been enabled the type of transition can be specified (rising or falling edge). Even when groups of DIO lines are configured as alternative functions such as the UARTs or Timers etc, any input line in the group can still be used to provide a wakeup event. This means that an external device communicating over the UART can wakeup a sleeping device by asserting its RTS signal pin (which is the CTS input of the JN5139).

16.3.3 Comparator Event

The comparator can generate a wakeup interrupt when a change in the relative levels of the positive and negative inputs occurs. The ability to wakeup when continuously monitoring analogue signals is useful in ultra-low power applications. For example, the JN5139 can remain in sleep mode until the voltage drops below a threshold and then be woken up to deal with the alarm condition.

16.4 Deep Sleep Mode

Deep sleep mode gives the lowest power consumption. All switchable power domains are off and certain functions in the VDD supply power domain, including the 32kHz system clock are stopped. This mode can be exited by a power down, a hardware reset on the RESETN pin, or a DIO event. The DIO event in this mode causes a chip reset to occur.

17 Electrical Characteristics

17.1 Maximum ratings

Exceeding these conditions may result in damage to the device.

Parameter		Min	Max
Device supply voltage VDD1, VDD2		-0.3V	3.6V
Supply voltage at voltage regulator bypass pins VB_xxx		-0.3V	1.98V
Voltage on analogue pins XTALOUT, XTALIN, VCOTUNE, RFP, RFM,		-0.3V	VB_xxx + 0.3V
Voltage on analogue pins VREF, ADC1-4, DAC1-2, COMP1M, COMP1P, COMP2M, COMP2P, IBIAS,		-0.3V	VDD1 + 0.3V
Voltage on 5v tolerant digital pins SPICLK, SPIMOSI, SPIMISO, SPISEL0, DIO0-DIO8, DIO11-DIO20, RESETN		-0.3V	Lower of (VDD2 + 2V) and 5.5V
Voltage on 3v tolerant digital pins DIO9, DIO10		-0.3V	VDD2 + 0.3V
Storage temperature		-40ºC	150ºC
Reflow soldering temperature according to IPC/JEDEC J-STD-020C			260ºC
ESD rating	Human Body Model [1]		2.0kV
	Machine Model [2]		200V
	Charged Device Model [3]		500V

1) Testing for Human Body Model discharge is performed as specified in JEDEC Standard JESD22-A114.
2) Testing for Machine Model discharge is performed as specified in JEDEC Standard JESD11-A115.
3) Testing for Charged Device Model discharge is performed as specified in JEDEC Standard JESD22-C101.

17.2 DC Electrical Characteristics

17.2.1 Operating Conditions

Supply	Min	Max
VDD1, VDD2	2.2V	3.6V
Ambient temperature range	-40ºC	85ºC

17.2.2 DC Current Consumption

VDD = 2.2 to 3.6V, -40 to +85º C

17.2.2.1 Active Processing

Mode:	Min	Typ	Max	Unit	Notes
CPU processing		2.85 + 0.295/MHz	4.5 + 0.480/MHz	mA	SPI, DIOs enabled, code executing in RAM (see 16.2)
Radio transmit [boost mode]		38 [42]	50 [55]	mA	CPU in software doze – radio transmitting
Radio receive [boost mode]		37 [40]	48 [53]	mA	CPU in software doze – radio in receive mode
The following current figures should be added to those above if the feature is being used					
ADC		655		µA	Temperature sensor and battery measurements require ADC
DAC		215 / 235		µA	One / both
Comparator		67.5 [1.2]		µA	Fast response time [low-power]
UART		95		µA	For each UART
Timer		65		µA	For each Timer
2-wire serial interface		75		µA	

17.2.2.2 Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Sleep mode with I/O wakeup (Waiting on I/O event)		0.1		µA	
Sleep mode with I/O and RC Oscillator timer wakeup – measured at 25ºC		1.2		µA	As above but also waiting on timer event. If both wakeup timers are enabled then add another 0.25µA
The following current figures should be added to those above if the feature is being used					
RAM retention – measured at 25ºC		2.4		µA	For full 96kB retained.
Comparator (low-power mode)		1.2		µA	Reduced response time.

17.2.2.3 Deep Sleep Mode

Mode:	Min	Typ	Max	Unit	Notes
Deep sleep mode – measured at 25ºC		60	250	nA	Waiting on chip RESET or I/O event.

17.2.3 I/O Characteristics

VDD = 2.2 to 3.6V, -40 to +85º C

Parameter	Min	Typ	Max	Unit	Notes
Internal DIO pull – up resistors	22 24 31	34 40 56	53 63 92	kΩ	VDD2 = 3.6V VDD2 = 3.0V VDD2 = 2.2V
Digital I/O High Input (excludes DIO9 and DIO10)	VDD2 x 0.7		Lower of (VDD2 + 2V) and 5.5V	V	5V Tolerant I/O only
Digital I/O High Input for DIO9 and DIO10	VDD2 x 0.7		VDD2	V	
Digital I/O low Input	-0.3		VDD x 0.27	V	
Digital I/O input hysteresis	140	230	310	mV	
DIO High O/P (2.7-3.6V)	VDD2 x 0.8		VDD2	V	With 4mA load
DIO Low O/P (2.7-3.6V)	0		0.4V	V	With 4mA load
DIO High O/P (2.2-2.7V)	VDD2 x 0.8		VDD2	V	With 3mA load
DIO Low O/P (2.2-2.7V)	0		0.4V	V	With 3mA load
Current sink/source capability		4 3		mA	VDD2 = 2.7V to 3.6V VDD2 = 2.2V to 2.7V
Input Leakage Current I_{IL}			50	nA	VDD = 3.6V, pin low
Input Leakage Current I_{IH}			50	nA	VDD = 3.6V, pin high

17.3 AC Characteristics

17.3.1 Reset

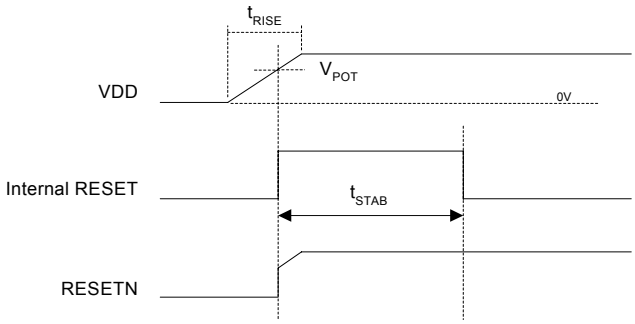


Figure 40: Power-on Reset

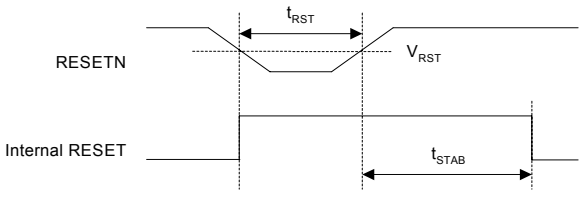


Figure 41: External Reset

VDD = 2.2 to 3.6V, -40 to +85º C

Parameter	Min	Typ	Max	Unit	Notes
External Reset pulse width (t_{RST})	1			µs	Assumes internal pullup resistor value of 100K worst case and ~5pF external capacitance
External Reset threshold voltage (V_{RST})	VDD2 x 0.7			V	Minimum voltage to avoid being reset
Internal Power-on Reset threshold voltage (V_{POT})		1.90 1.95 2.00		V	VDD2 = 2.2V VDD2 = 3.0V VDD2 = 3.6V Note 1
Power rise time (t_{RISE})			1	ms	See section 6
Reset stabilisation time (t_{STAB})		2.75		ms	Note 2

[1] VDD rise time of 1ms and 25 deg C

[2] Time from release of reset to start of executing ROM code. Loading program from Flash occurs in addition to this.

17.3.2 SPI Master Timing

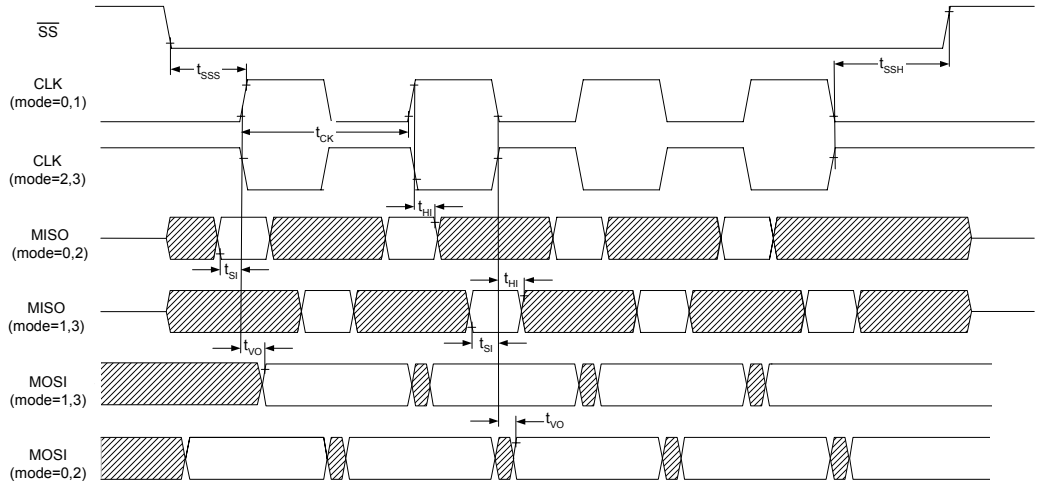


Figure 42: SPI Timing (Master)

Parameter	Symbol	Min	Max	Unit
Clock period	t_{CK}	62.5	-	ns
Data setup time	t_{SI}	15.3 @ 2.7-3.6V 30.5 @ 2.2-3.6V	-	ns
Data hold time	t_{HI}	0		ns
Data invalid period	t_{VO}	-	15	ns
Select set-up period	t_{SSS}	55	-	ns
Select hold period	t_{SSH}	25 (SPICLK = 16MHz) 0 (SPICLK<16MHz, mode=0 or 2) 55 (SPICLK<16MHz, mode=1 or 3)	-	ns

17.3.3 Intelligent Peripheral (SPI Slave) Timing

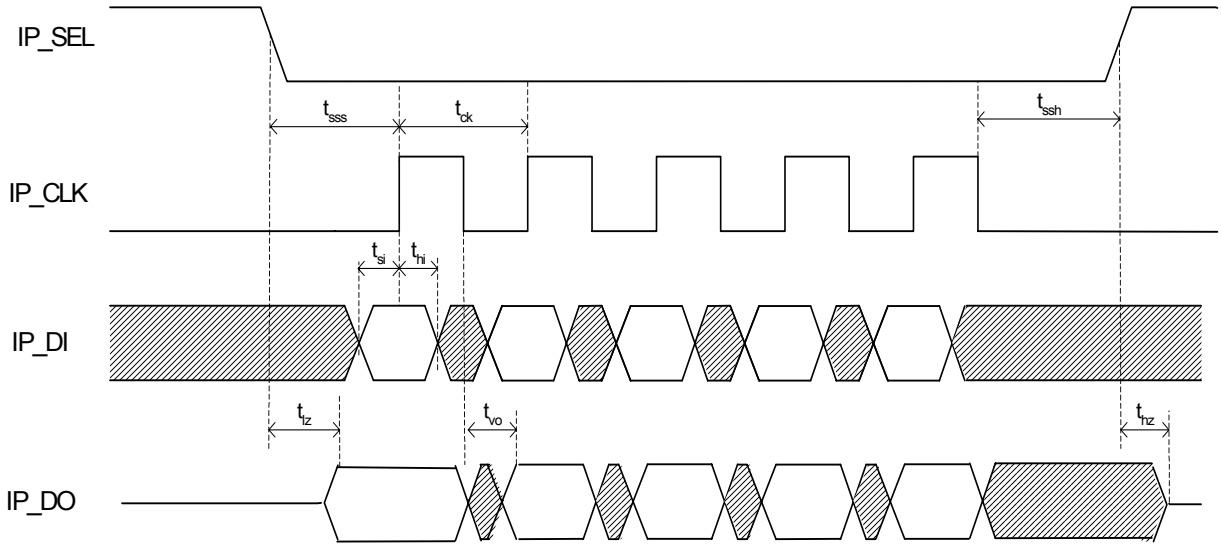


Figure 43: Intelligent Peripheral (SPI Slave) Timing

Parameter	Symbol	Min	Max	Unit
Clock period	t_{ck}	125.0	-	ns
Data setup time	t_{si}	15	-	ns
Data hold time	t_{hi}	15		ns
Data invalid period	t_{vo}	-	40	ns
Select set-up period	t_{sss}	15	-	ns
Select hold period	t_{ssh}	15	-	ns
Select asserted to output data driven	t_{lz}		20	ns
Select negated to data output tri-stated	t_{hz}		20	ns

17.3.4 Two-wire serial interface

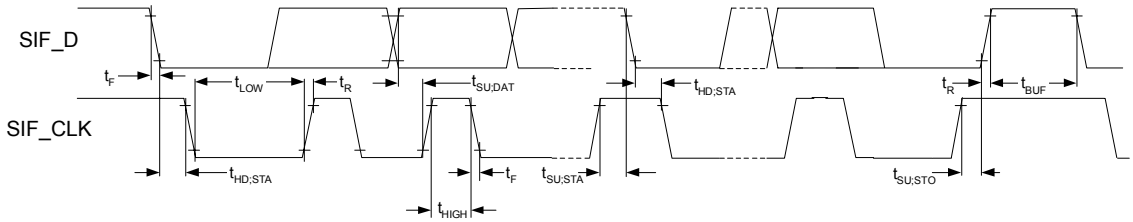


Figure 44: Two-wire serial Interface Timing

Parameter	Symbol	Standard Mode		Fast Mode		Unit
		Min	Max	Min	Max	
SIF_CLK clock frequency	f_{SCL}	0	100	0	400	kHz
Hold time (repeated) START condition. After this period, the first clock pulse is generated	$t_{HD:STA}$	4	-	0.6	-	µs
LOW period of the SIF_CLK clock	t_{LOW}	4.7	-	1.3	-	µs

HIGH period of the SIF_CLK clock	t_{HIGH}	4	-	0.6	-	µs
Set-up time for repeated START condition	$t_{SU:STA}$	2	-	0.5	-	µs
Data setup time SIF_D	$t_{SU:DAT}$	0.25	-	0.1	-	µs
Rise Time SIF_D and SIF_CLK	t_R	-	1000	20+0.1Cb	300	ns
Fall Time SIF_D and SIF_CLK	t_F	-	300	20+0.1Cb	300	ns
Set-up time for STOP condition	$t_{SU:STO}$	4	-	0.6	-	µs
Bus free time between a STOP and START condition	t_{BUF}	4.7	-	1.3	-	µs
Capacitive load for each bus line	C_b	-	400	-	400	pF
Noise margin at the LOW level for each connected device (including hysteresis)	V_{nl}	0.1VDD	-	0.1VDD	-	V
Noise margin at the HIGH level for each connected device (including hysteresis)	V_{nh}	0.2VDD	-	0.2VDD	-	V

17.3.5 Power Down and Wake-Up timings

Parameter	Min	Typ	Max	Unit	Notes
Wake up from Deep Sleep (or reset)		2.75 + 0.5* program size in kBytes		ms	Assumes SPI clock to external Flash is16MHz
Wake up from Sleep (memory not held)		2.75 + 0.5* program size in kBytes		ms	Assumes SPI clock to external Flash is16MHz
Wake up from Sleep (Memory held)		2.75		ms	
Wake up from CPU Doze mode		0.2		µs	

Note: The 2.75ms time is from release of reset or the wakeup event to the CPU executing code. At this point if the Flash is read there is an additional startup delay, as shown in the table.

17.3.6 32kHz Oscillator

VDD = 2.2 to 3.6V, -40 to +85 ºC

Parameter	Min	Typ	Max	Unit	Notes
Current consumption of cell and counter logic		1.2 1.0 0.8		µA	3.6V 3.0V 2.2V
32kHz clock native accuracy	-30%	32kHz	+30%		Typical at 3.0V 25°C
Calibrated 32kHz accuracy		±330		ppm	For a 1 second sleep period calibrating over 20 x 32kHz clock periods
Variation with temperature		+0.008		%/°C	
Variation with VDD2		-5		%/V	

17.3.7 16MHz Crystal Oscillator

VDD = 2.2 to 3.6V, -40 to +85ºC

Parameter	Min	Typ	Max	Unit	Notes
Current consumption	80	215	350	µA	Including bandgap ref.
Start – up time		2.75		ms	Assuming xtal with ESR of 40ohms and CL= 9pF External caps = 15pF (150mV pk-pk) see Appendix B
Input capacitance		1.4		pF	Bondpad and package, guaranteed by design
Transconductance	1.05	1.30	1.70	mA/V	
DC voltages, XTALIN, XTALOUT	300	390	480	mV	
External Capacitors		15		pF	CL = 9pF, total external capacitance needs to be 2*CL, allowing for stray capacitance from chip, package and PCB

17.3.8 Bandgap Reference

VDD = 2.2 to 3.6V, -40 to +85ºC

Parameter	Min	Typ	Max	Unit	Notes
Voltage	1.134	1.176	1.217	V	
DC power supply rejection		-58		dB	at 25ºC
Temperature coefficient		-82 +40		ppm/°C	0 to 85ºC -40ºC to 0ºC
Point of inflexion		0		ºC	

17.3.9 Analogue to Digital Converters

VDD = 3.0V, VREF = 1.2V, -40 to +85ºC

Parameter	Min	Typ	Max	Unit	Notes
Resolution			12	bits	500kHz Clock
Current consumption		655		µA	
Integral nonlinearity		± 5		LSB	0 to Vref range
Differential nonlinearity	-1		+2	LSB	Guaranteed monotonic
Offset error		+10		mV	
Gain error		-20		mV	
Internal clock		500		kHz	16MHz input clock, ÷32
No. internal clock periods to sample input		2, 4, 6 or 8			Programmable
Conversion time	40			µs	500KHz Clock with sample period of 2
Input voltage range	0.04		Vref or 2*Vref	V	Switchable. Refer to 15.1.1
Vref (Internal)	See Section 17.3.8 Bandgap Reference				
Vref (External)	1.15	1.2	1.6	V	Allowable range into VREF pin
Input capacitance		8		pF	In series with 5K ohms

17.3.10 Digital to Analogue Converters

VDD = 3.0V, VREF = 1.2V, -40 to +85ºC

Parameter	Min	Typ	Max	Unit	Notes
Resolution		11		bits	
Current consumption		215 (single) 235 (both)		µA	
Integral nonlinearity		±2		LSB	
Differential nonlinearity	-1		+1	LSB	Guaranteed monotonic
Offset error		±10		mV	
Gain error		±10		mV	
Internal clock		2MHz, 1MHz, 500kHz, 250kHz			16MHz input clock, programmable prescaler
Output settling time to 0.5LSB		5		µs	With 10k ohms & 20pF load
Minimum Update time	10			µs	2MHz Clock with sample period of 8
Output voltage swing	0	Lower of Vdd-1.2 and Vref		V	Output voltage swing Gain =0
Output voltage swing	0	Lower of 2x(Vdd-1.2) and Vdd-0.2 and 2xVref		V	Output voltage swing Gain =1
Vref (Internal)	See Section 17.3.8 Bandgap Reference				
VREF (External)	0.8	1.2	1.6	V	Allowable range into VREF pin
Resistive load	10			kΩ	To ground
Capacitive load			20	pF	
Digital input coding	Binary				

17.3.11 Comparators

VDD = 2.2 to 3.6V -40 to +85ºC

Parameter	Min	Typ	Max	Unit	Notes
Analogue response time (normal)		105	140	ns	+/- 250mV overdrive 10pF load
Total response time (normal) including delay to Interrupt controller			105 + 125	ns	Digital delay can be up to a max. of two 16MHz clock periods
Analogue response time (low power)		2.4		µs	+/- 250mV overdrive No digital delay
Hysteresis	4 12 28	10 20 40	16 26 50	mV	Programmable in 3 steps and zero.
Vref (Internal)	See Section 17.3.8 Bandgap Reference			V	
Common Mode input range	0		Vdd	V	
Current (normal mode)	40	67.5	90	µA	
Current (low power mode)		1.2		µA	

17.3.12 Temperature Sensor

Parameter	Min	Typ	Max	Unit	Notes
Operating Range	-40	-	85	°C	
Sensor Gain	-1.44	-1.55	-1.66	mV/°C	
Accuracy	-	-	±10	°C	
Non-linearity	-	-	2.5	°C	
Output Voltage	630	745	855	mV	Includes absolute variation due to manufacturing & temp
Typical Voltage		745		mV	Typical at 3.0V 25°C
Resolution	0.154	0.182	0.209	°C/LSB	0 to Vref ADC I/P Range

17.3.13 Radio Transceiver

The JN5139 meets all the requirements of the IEEE802.15.4 standard for 2.2-3.6V and offers the following improved RF characteristics. All RF characteristics are measured single ended and include the losses of a ceramic balun.

This part also meets the following regulatory body approvals, when used with Jennic's Module Reference Designs. Compliant with FCC part 15, rules, IC Canada, ETSI ETS 300-328 and Japan ARIB STD-T66

Parameter	Min	Typical	Max	Notes
RF Port Characteristics				
Type				Differential
Impedance		200ohm		2.4-2.5GHz
Frequency range	2.400 GHz		2.485GHz	

17.3.13.1 Radio parameters: 2.2-3.6V, +25ºC

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity	-92	-96		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Receive sensitivity (boost)	-92.5	-96.5		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Maximum input signal			+10	dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection -1 channel / +1 channel [CW Interferer]		31 / 35 [35 / 38]		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1) (modulated interferer)
Alternate channel rejection [CW Interferer]		42 [45]		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1) (modulated interferer)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		50		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		47		dB	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 4dB lower. (Note1)
Spurious emissions (RX)		 -69 -53	 -65 -50	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		50		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm
Transmitter Characteristics					
Transmit power	-2.5	+1.5		dBm	
Transmit power (boost)	0	+2.7		dBm	
Output power control range		-31.5		dB	In five 6dB steps (Note2)
Spurious emissions (TX)		 -66 -41 -72	 -63 -38	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz

Parameter	Min	Typical	Max	Unit	Notes
EVM [offset]		15 [4.5]	25	%	At maximum output power
Transmit Power Spectral Density		-37	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, section 6.5.3.1

17.3.13.2 Radio parameters: 2.2-3.6V, -40ºC

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity		-97		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Maximum input signal			+10	dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection -1 channel / +1 channel		31 / 35		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Alternate channel rejection		42		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		45		dB	For 1% PER with wanted signal 3dB above sensitivity. (Note1)
Out of band rejection		47		dB	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 4dB lower. (Note1)
Spurious emissions (RX)		 -69 -53	 -64 -50	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1 to 12GHz
Intermodulation protection		50		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm
Transmitter Characteristics					
Transmit power		+2		dBm	
Transmit power (boost)		+3		dBm	
Output power control range		-31.0		dB	In five 6dB steps (Note2)
Spurious emissions (TX)		 -64 -38 -72	 -61 -35	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to12.5GHz, The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz

Parameter	Min	Typical	Max	Unit	Notes
EVM [offset]		20 [6.2]	30	%	At maximum output power
Transmit Power Spectral Density		-36	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, section 6.5.3.1

17.3.13.3 Radio parameters: 2.2-3.6V, +85ºC

Parameter	Min	Typical	Max	Unit	Notes
Receiver Characteristics					
Receive sensitivity		-94		dBm	Nominal for 1% PER, as per 802.15.4 section 6.5.3.3
Maximum input signal			+10	dBm	For 1% PER, measured as sensitivity
Adjacent channel rejection -1 channel / +1 channel		27 / 35		dB	For 1% PER with wanted signal 3dB above sensitivity, (Note1)
Alternate channel rejection		42		dB	For 1% PER with wanted signal 3dB above sensitivity, (Note1)
Other in band rejection 2.4 to 2.4835 GHz, excluding adj channels		50		dB	For 1% PER with wanted signal 3dB above sensitivity, (Note1)
Out of band rejection		47		dB	For 1% PER with wanted signal 3dB above sensitivity. All frequencies except wanted/2 which is 4dB lower (Note1)
Spurious emissions (RX)		 -69 -54	 -66 -51	dBm	Measured conducted into 50ohms 30MHz to 1GHz 1GHz to 12GHz
Intermodulation protection		51		dB	For 1% PER at with wanted signal 3dB above sensitivity. Modulated Interferers at 2 & 4 channel separation. (Note1)
RSSI linearity	-4		+4	dB	-95 to -10dBm
Transmitter Characteristics					
Transmit power		-1.3		dBm	
Transmit power (boost)		+0.6		dBm	
Output power control range		-32.0		dB	In five steps of 6dB (Note2)
Spurious emissions (TX)		 -69 -44	 -66 -41	dBm	Measured conducted into 50ohms 30MHz to 1GHz, 1GHz to12.5GHz,

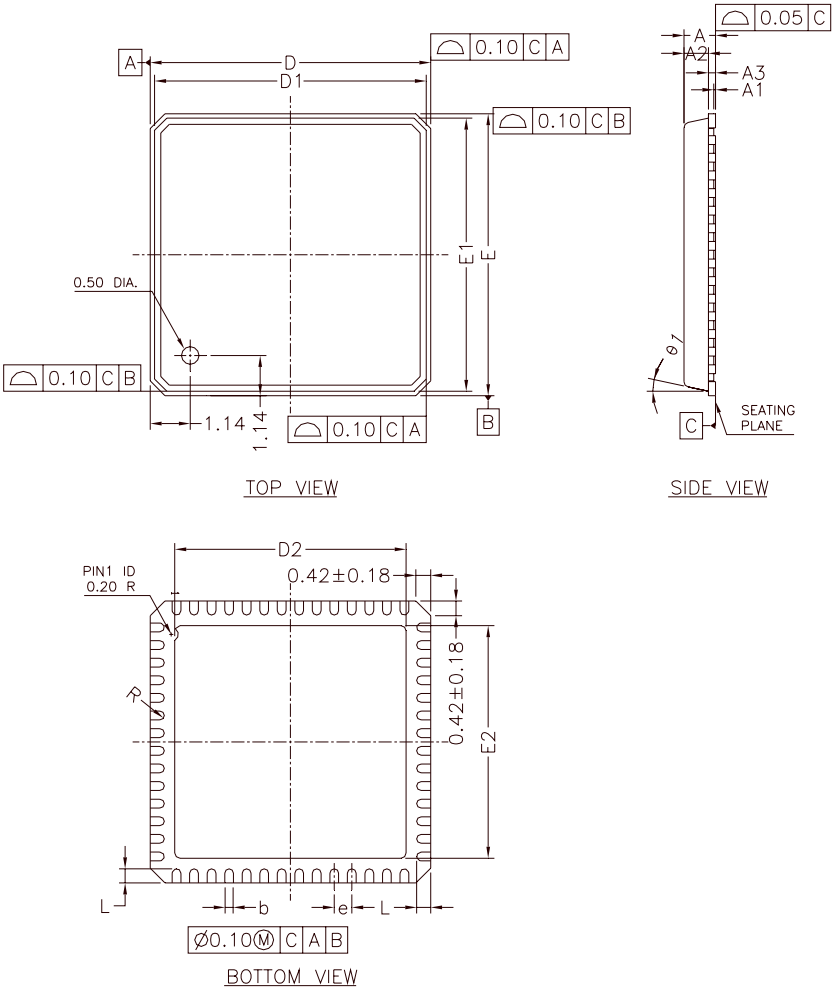
Parameter	Min	Typical	Max	Unit	Notes
		-72			The following exceptions apply 1.8 to 1.9GHz & 5.15 to 5.3GHz
EVM [offset]		12 [3.6]	25	%	At maximum output power
Transmit Power Spectral Density		-38	-20	dBc	At greater than 3.5MHz offset, as per 802.15.4, section 6.5.3.1

Note1: Blocker rejection is defined as the value, when 1% PER is seen with the wanted signal 3dB above sensitivity, as per 802.15.4 section 6.5.3.4

Note2: Up to an extra 4dB of attenuation is available if required.

Appendix A Mechanical and Ordering Information

A.1 56pin QFN Package Drawing

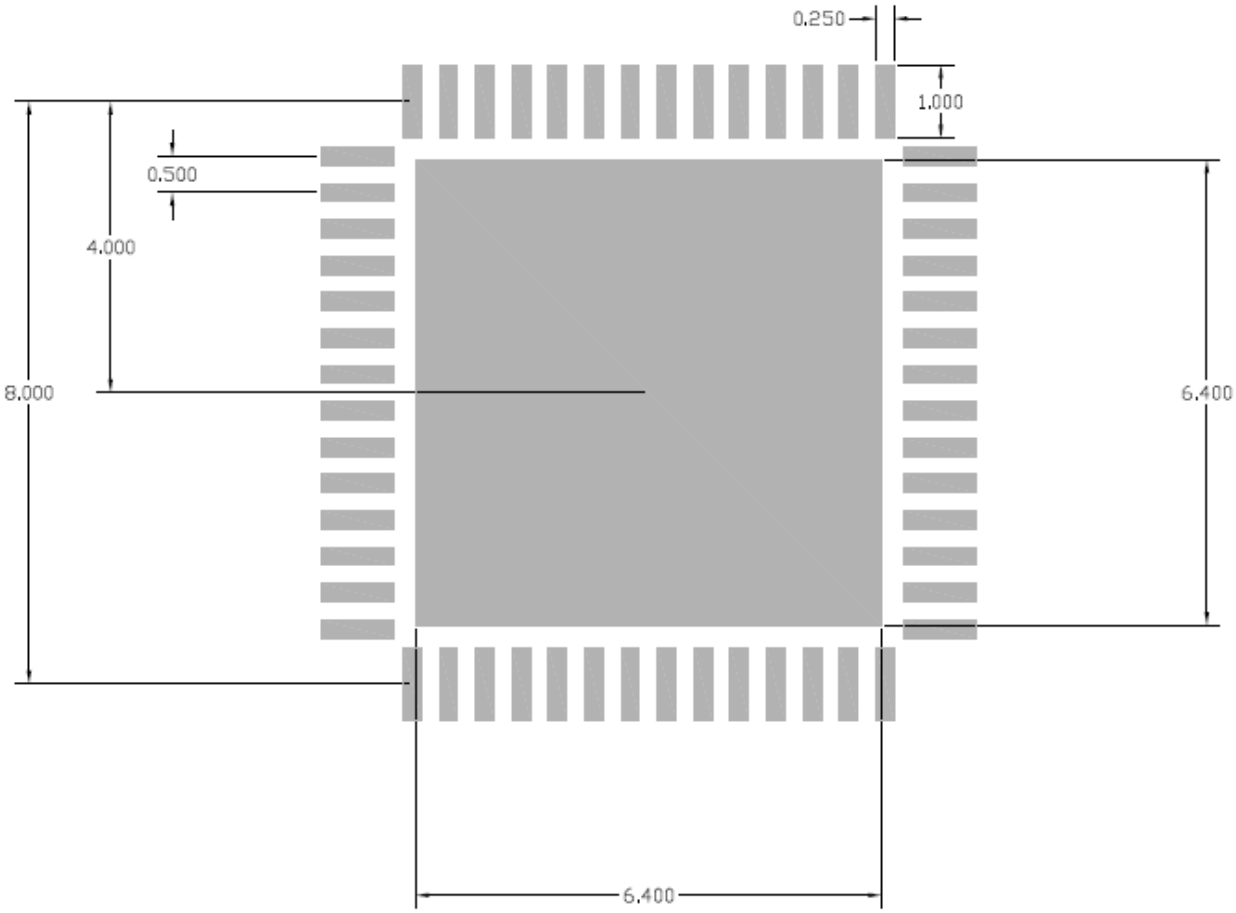


Controlling Dimension: mm

Symbol	millimetres		
	Min.	Nom.	Max.
A	------	------	0.9
A1	0.00	0.01	0.05
A2	------	0.65	0.7
A3		0.20 Ref.	
b	0.2	0.25	0.3
D		8.00 bsc	
D1		7.75 bsc	
D2	6.20	6.40	6.60
E		8.00 bsc	
E1		7.75 bsc	
E2	6.20	6.40	6.60
L	0.30	0.40	0.50
e		0.50 bsc	
υ1	0°	------	12°
R	0.09	------	------
Tolerances of Form and Position			
aaa		0.10	
bbb		0.10	
ccc		0.05	

A.2 PCB Decal

The following PCB decal is recommended; all dimensions are in millimetres (mm).



For further detail please consult the Module Development Reference Manual JN-RM-2006, available to download from the Jennic Support web site **(www.jennic.com/support)**

A.3 Ordering Information

The standard qualification for the JN5139 is Industrial Specification: -40ºC to +85ºC, packaged in a 56-pin QFN (Quad Flat No-leads) package.

Ordering Format:

JN5139 – XXX - Y_1

Part Numbers:

JN5139 Wireless microcontroller - 96kB RAM

XXX: ROM Variant:

001 IEEE802.15.4

Z01 ZigBee

Y_1: Shipping:

T Tape mounted 2500 devices on a 330mm reel

V Tape mounted 1000 devices on a 180mm reel

X Tape mounted 500 devices on a 180mm reel

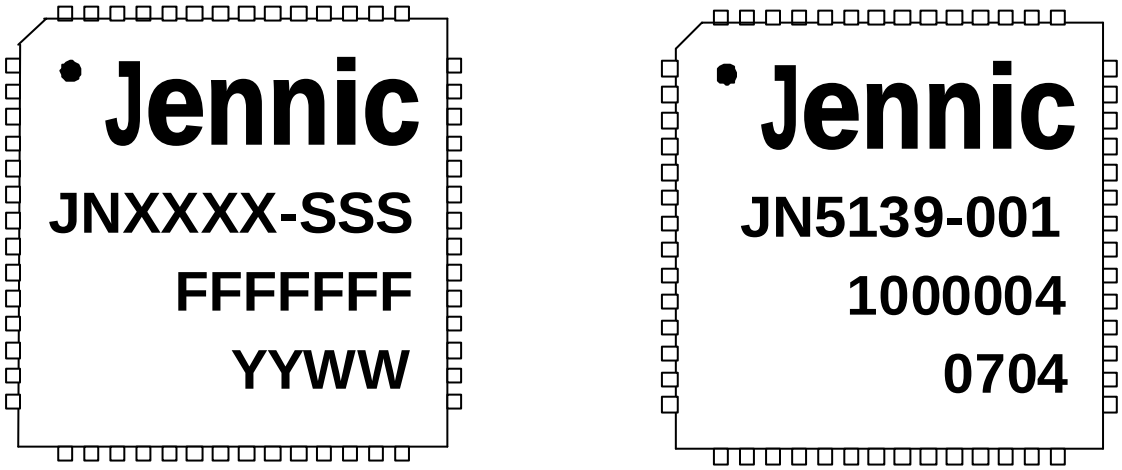
Y Tape mounted up to 500 devices (no reel, not dry packed)

Ordering Examples:

Part Number	Description
JN5139-001-X	JN5139 IEEE802.15.4 Wireless Microcontroller – 500 devices on a 180mm reel
JN5139-Z01-V	JN5139 ZigBee Microcontroller - 1000 devices on a 180mm reel

A.4 Device Package Marking

The diagram below shows the package markings for JN5139 devices. The package on the left along with the legend information below it, shows the general format of package marking. The package on the right shows the specific markings for a JN5139-001 device, that came from assembly build number 1000004 and was manufactured week 4 of 2007.



Legend:

JN	Jennic
XXXX	4 digit part number, for example 5139
SSS	3 digit software ROM identifier
FFFFFFF	7 digit assembly build number
YY	2 digit year number
WW	2 digit week number

Where this Data Sheet is denoted as “Advanced” or “Preliminary”, devices will be either Engineering or Prototype Samples. Devices of this status have an R suffix after the software ROM identifier, for example JN5139-001**R**.

Devices may also have an additional digit immediately after the R suffix, for example R**1**, R**2**, R**3** etc. This additional digit is use to identify different revisions of engineering or prototype silicon during these product phases.

A.5 Tape and Reel Information

A.5.1 Tape Orientation and Dimensions

The general orientation of the 56QFN package in the tape is as shown in Figure 45.

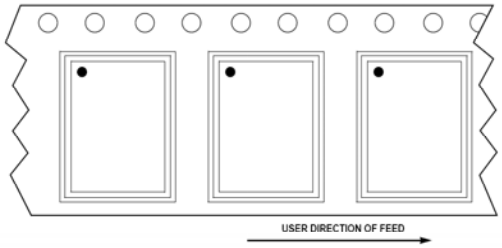
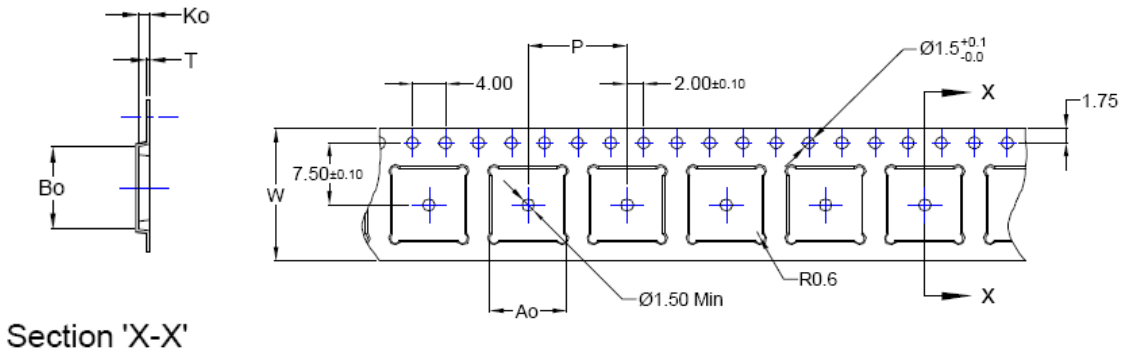


Figure 45: Tape and Reel Orientation

Figure 46 shows the detailed dimensions of the tape used for 8x8mm 56QFN devices.



Reference	Dimensions (mm)
A_o	8.30 ±0.10
B_o	8.30 ±0.10
K_o	1.10 ±0.10
P	12.00 ±0.10
T	0.30 ±0.10
W	16.00 +0.30/-0.10

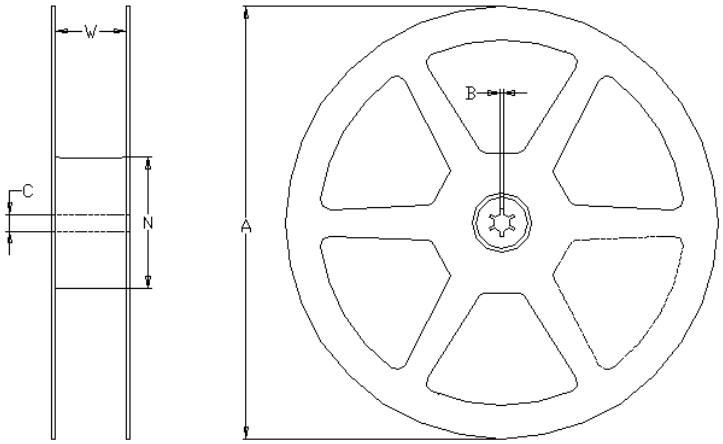
Figure 46: Tape Dimensions

A.5.2 Reel Information: 180mm Reel

Surface Resistivity	Between $10e^{9}$ – $10e^{11}$ Ohms Square
Material	High Impact Polystyrene, environmentally friendly, recyclable

All dimensions and tolerances are fully compliant with EIA-481-B and are specified in millimetres.

6 window design with one window on each side blanked to allow adequate labelling space.



Tape Width	A	B (min)	C	N	W (min)	W (max)
16	180	1.5min	13 ±0.2	60 +0.1 –0.0	16.40	17.90

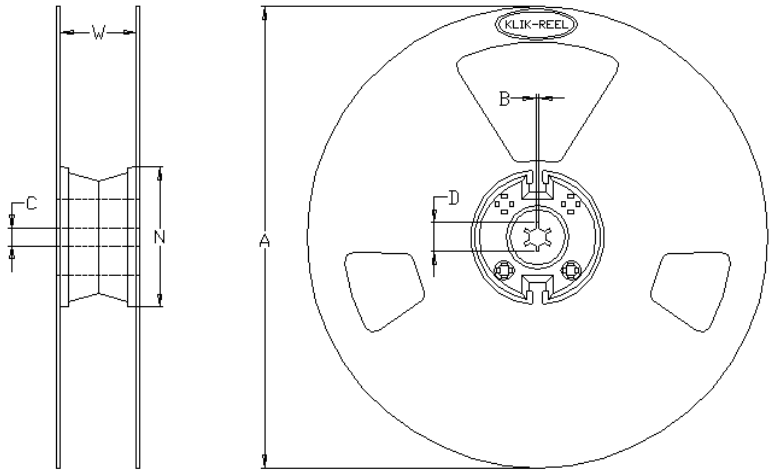
Figure 47: Reel Dimensions

A.5.3 Reel Information: 330mm Reel

Surface Resistivity	Between $10e^{9}$ – $10e^{11}$ Ohms Square
Material	High Impact Polystyrene with Antistatic Additive

All dimensions and tolerances are fully compliant with EIA-481-B and are specified in millimetres.

3 window design to allow adequate labelling space.



Tape Width	A	B (min)	C	D (min)	N (min)	W (min)	W (max)
16	330	1.5	13 +0.5 -0.2	20.2	100	15.90	19.40

A.5.4 Dry Pack Requirement for Moisture Sensitive Material

Moisture sensitive material, as classified by JEDEC standard J-STD-033, must be dry packed. The 56 lead QFN package is MSL2A/260°C, and is dried before sealing in a moisture barrier bag (MBB) with desiccant bag weighing at 67.5 grams of activated clay and a 6 spot humidity indicator card (HIC) meeting MIL-L-8835 specification. The MBB has a moisture-sensitivity caution label to indicate the moisture-sensitive classification of the enclosed devices.

A.6 PCB Design and Reflow Profile

PCB and land pattern designs are key to board level reliability, and Jennic strongly recommends that users follow the design rules listed in IPC-SM-782. For reflow profiles, it is recommended to follow the reflow profile in Figure 48 as a guide, as well as the paste manufacturers guidelines on peak flow temperature, soak times, time above liquidus and ramp rates.

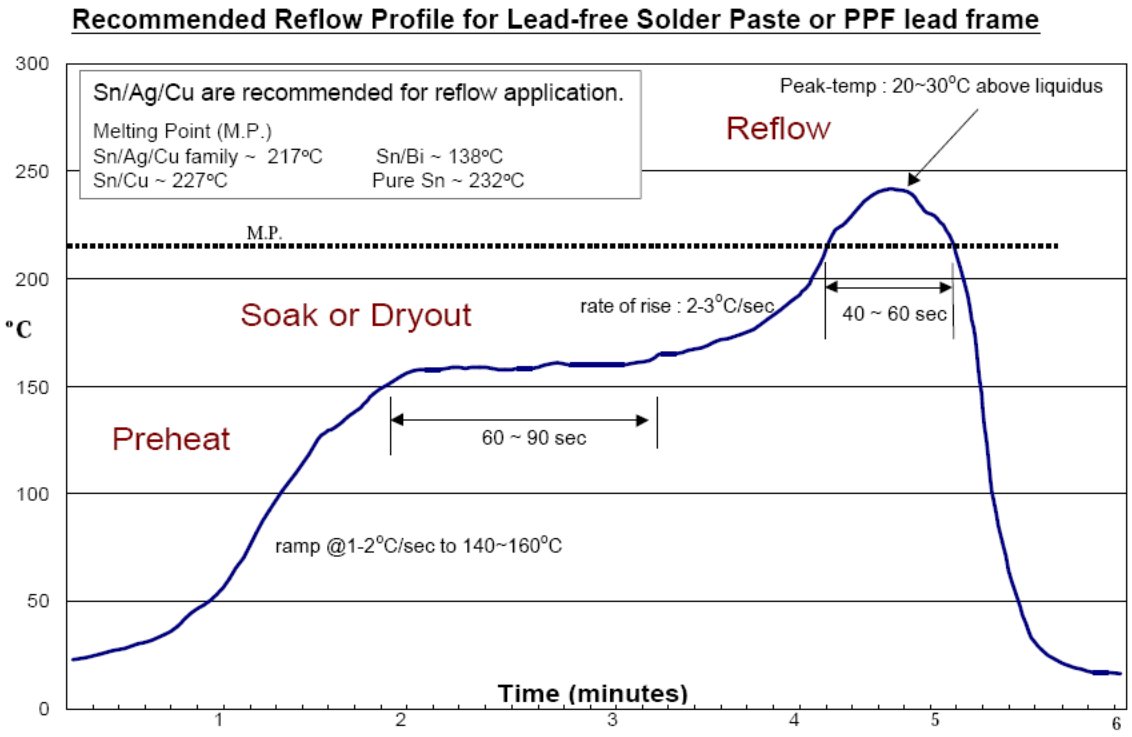


Figure 48: Reflow Profile

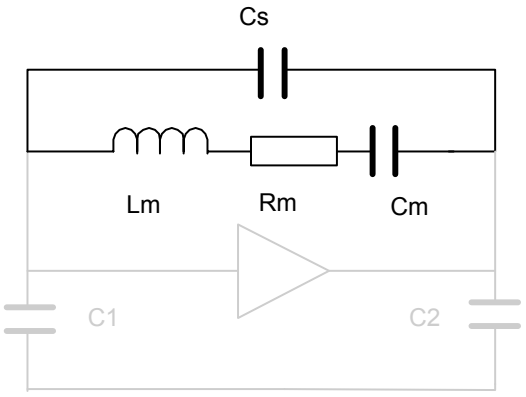
Appendix B Development Support

B.1 Crystal Oscillator

16MHz Crystal Requirements

Parameter	Min	Typ	Max	Notes
Crystal Frequency		16MHz		
Crystal Tolerance			40ppm	Including temperature and ageing
Crystal ESR Range (Rm)	10Ω		60Ω	See below for more details
Crystal Load Capacitance Range (CL)	6pF	9pF	12pF	See below for more details
Not all Combinations of Crystal Load Capacitance and ESR are valid refer to Section B.1.3				
Recommended Crystal	Load Capacitance 9pF and max ESR 40 Ω			
External Capacitors (C1 & C2) For recommended Crystal		15pF		CL = 9pF, total external capacitance needs to be 2*CL. , allowing for stray capacitance from chip, package and PCB

B.1.1 Crystal Equivalent Circuit



Where C_m is the motional capacitance

L_m is the motional inductance. This together with C_m defines the oscillation frequency (series)

R_m is the equivalent series resistance (ESR).

C_S is the shunt or package capacitance and this is a parasitic

B.1.2 Crystal Load Capacitance

The crystal load capacitance is the total capacitance seen at the crystal pins, from all sources. As the load capacitance (CL) affects the oscillation frequency by a process known as 'pulling', crystal manufacturers specify the frequency for a given load capacitance only. A typical pulling coefficient is 15ppm/pF, to put this into context the maximum frequency error in the IEEE802.15.4 specification is +/-40ppm for the transmitted signal. Therefore, it is important for resonance at 16MHz exactly, that the specified load capacitance is provided.

The load capacitance can be calculated using:

$$CL = \frac{C_{T1} \times C_{T2}}{C_{T1} + C_{T2}}$$

Total capacitance $$C_{T1} = C_1 + C_{1P} + C_{1in}$$

Where C_1 is the capacitor component

C_{1P} is the PCB parasitic capacitance. With the recommended layout this is about 1.6pF

C_{1in} is the on-chip parasitic capacitance and is about 1.4pF typically.

Similarly for C_{T2}

Hence for a 9pF load capacitance, and a tight layout the external capacitors should be 15pF

B.1.3 Crystal ESR and Required Transconductance

The resistor in the crystal equivalent circuit represents the energy lost. To maintain oscillation, power must be supplied by the amplifier, but how much? Firstly, the Pi connected capacitors C_1 and C_2 with C_S from the crystal, apply an impedance transformation to Rm, when viewed from the amplifier. This new value is given by:

$$\hat{R}_m = R_m\left(\frac{C_S + C_L}{C_L}\right)^2$$

The amplifier is a transconductance amplifier, which takes a voltage and produces an output current. The amplifier together with the capacitors C1 and C2, form a circuit, which provides a negative resistance, when viewed from the crystal. The value of which is given by:

$$R_{NEG} = \frac{g_m}{C_{T1} \times C_{T2} \times \omega^2}$$

Where g_m is the transconductance

ω is the frequency in rad/s

Derivations of these formulas can be easily found in textbooks.

In order to give quick and reliable oscillator start-up, a common rule of thumb is to set the amplifier negative resistance to be a minimum of 4 times the effective crystal resistance. This gives

$$\frac{g_m}{C_{T1} \times C_{T2} \times \omega^2} \geq 4R_m\left(\frac{C_S + C_L}{C_L}\right)^2$$

This can be used to give an equation for the required transconductance.

$$g_m \geq \frac{4R_m \times \omega^2 [C_S(C_{T1}+C_{T2})+C_{T1}\times C_{T2}]^2}{C_{T1}\times C_{T2}}$$

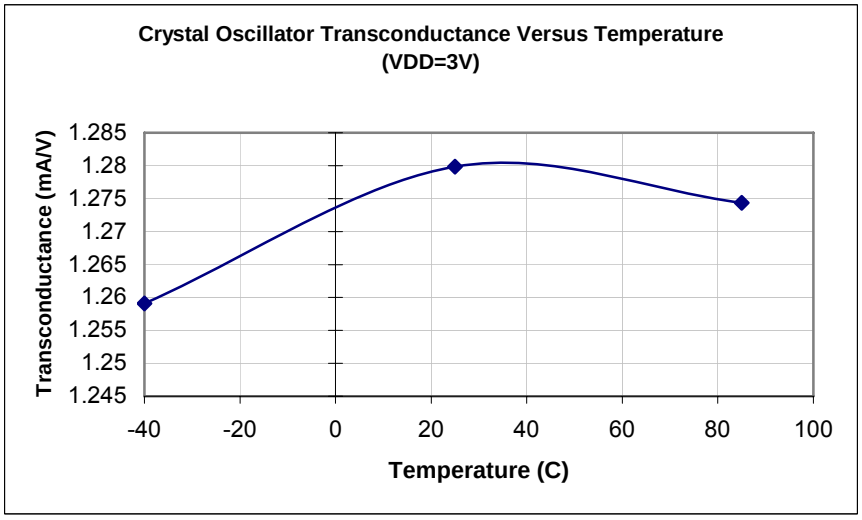
Example: Using typical parameters of R_m =40Ω, C_S =1pF and $C_{T1} = C_{T2}$ =18pF (for a load capacitance of 9pF), the equation above gives the required transconductance (g_m) as 647uA/V. The JN5139 has a typical value for transconductance of 1.25mA/V

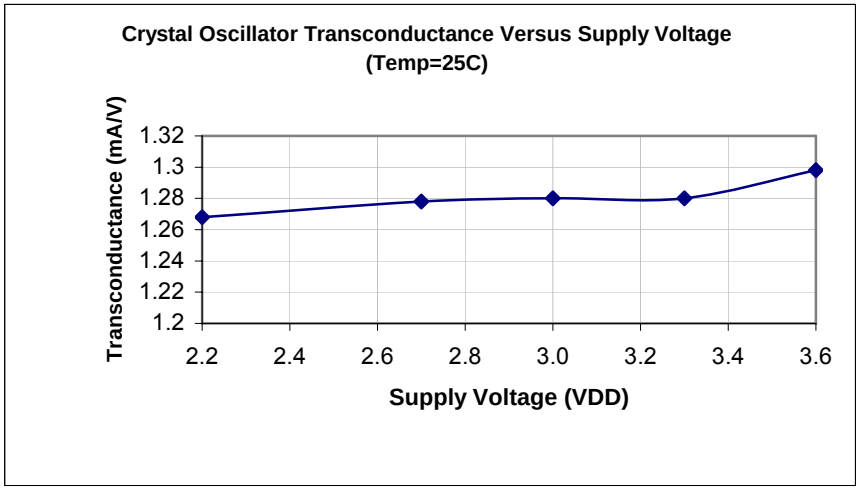
The example and equation illustrate the trade-off that exists between the load capacitance and crystal ESR. For example, a crystal with a higher load capacitance can be used, but the value of max. ESR that can be tolerated is reduced. Also note, that the circuit sensitivity to external capacitance [C_1 , C_2] is a square law.

Meeting the criteria for start-up is only one aspect of the way these parameters affect performance, they also affect the time taken during start-up to reach a given, (or full), amplitude. Unfortunately, there is no simple mathematical model for this, but the trend is the same. Therefore, both a larger load capacitance and larger crystal ESR will give a longer start-up time, which has the disadvantages of reduced battery life and increased latency.

For this reason, we strongly recommend that for a 9pF load capacitance crystals be specified with a maximum ESR of 40 ohms. For lower load capacitances the recommended maximum ESR rises, for example, CL=7pF the max ESR is 61 ohms. For the lower cost crystals in the large HC49 package, a load capacitance of 10pF is widely available and the max ESR of 30 ohms specified by many manufacturers is acceptable. Also available in this package style, are crystals with a load capacitance of 12pF, but in this case the max ESR required is 25 ohms or better.

Below is measurement data showing the variation of the crystal oscillator amplifier transconductance with temperature and supply voltage, notice how small the variation is. Circuit techniques have been used to apply compensation, such that the user need only design for nominal conditions.





B.2 16MHz Oscillator

The JN5139 contains the necessary on-chip components to build a 16 MHz reference oscillator with the addition of an external crystal resonator, two tuning capacitors and a resistor. The schematic of these components are shown in Figure 49. The two capacitors, C1 and C2, will typically be 15pF ±5% and use a COG dielectric, R2 should be 1M5Ω. For a detailed specification of the crystal required and factors affecting C1 and C2 see Appendix B.1. As with all crystal oscillators the PCB layout is especially important, both to keep parasitic capacitors to a minimum and to reduce the possibility of PCB noise being coupled into the oscillator.

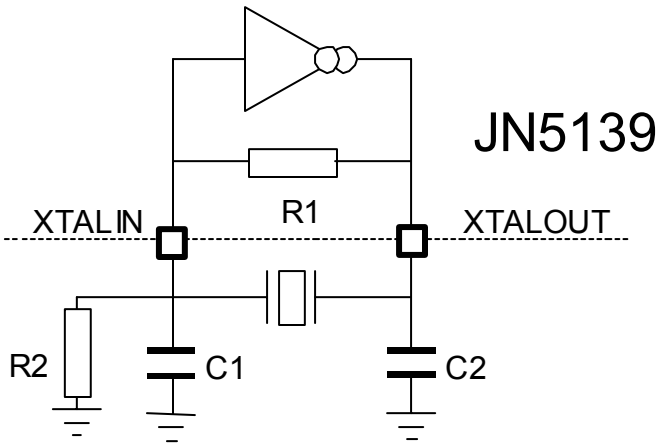


Figure 49: Crystal oscillator connections

The clock generated by this oscillator provides the reference for most of the JN5139 subsystems, including the transceiver, processor, memory and digital and analogue peripherals.

B.3 Applications Information

B.3.1 Typical Application Schematic

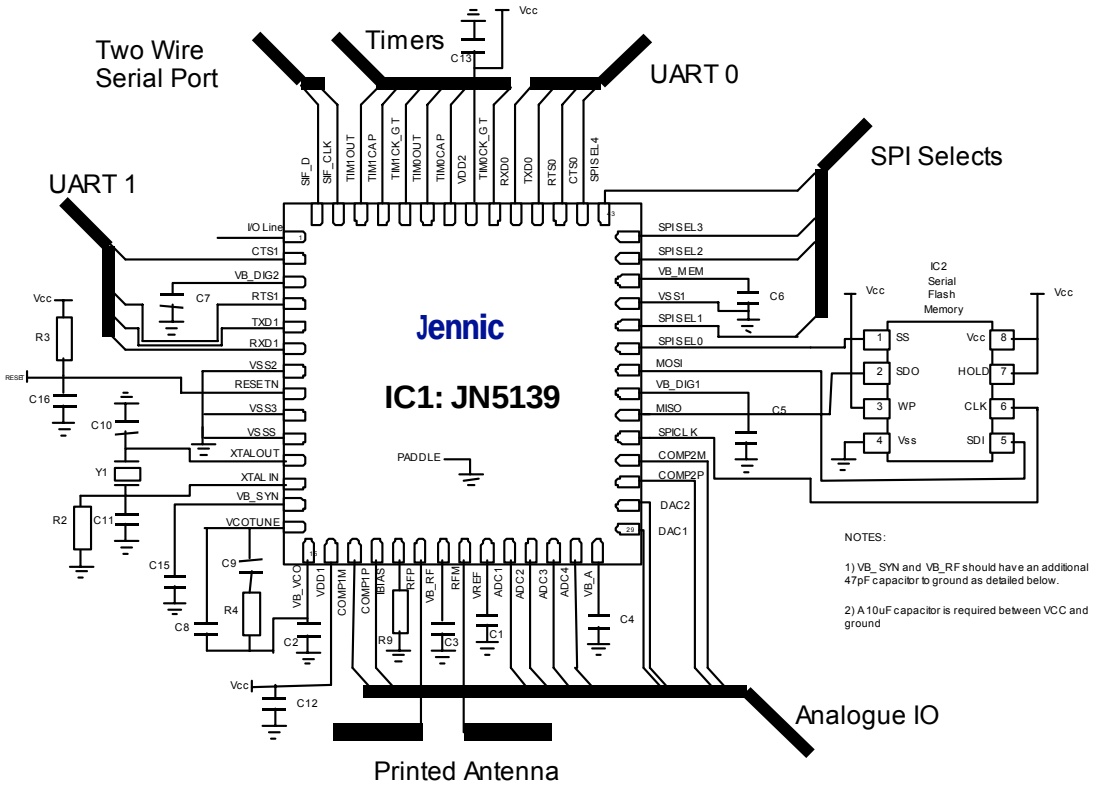


Figure 50: Application Schematic

Components	Values
C1, C2, C3, C4, C5, C6, C7, C12, C13, C15	100nF 5%
C10, C11	15pF 5% (COG)
C9	3n3F 5%
C8	330pF 5% (COG)
R4	4k7Ω 1%
R9	43kΩ 1%
Y1	TSX4025 16MHz Crystal - 9pF load capacitance
IC1	JN5139
IC2	128kB Serial Flash see section 4.4
C16	470nF 5%
R3	18kΩ 5%
VB_SYN, VB_RF (See Schematic Notes)	47pF NPO
R2	1.5MΩ 5%

Table 6: Bill of Materials

B.3.2 Reference Designs

For customers wishing to integrate the JN5139 device directly into their system, Jennic provide a range of Module Reference Designs, covering standard and high-power modules fitted with different Antennae.

These reference designs should be followed accurately to ensure the device operates as specified.

For further detail please consult the Module Development Reference Manual JN-RM-2006, available to download from the Jennic Support web site **(www.jennic.com/support)**

Appendix C

Related Documents

[1] IEEE Std 802.15.4-2003 IEEE Standard for Information technology – Part 15.4 Wireless Medium Access Control (MAC) and Physical Layer (PHY) Specifications for Low-Rate Wireless Personal Area Networks (LR-WPANs)

[2] JN-AN-1003 Boot Loader Operation

[3] JN-AN-1062 Using OTP eFuse Memory

[4] JN-AN-1038 Programming Flash devices not supported by the JN51xx ROM-based bootloader

[5] JN-RM-2001 Integrated Peripherals API Reference Manual

[6] JN-RM-2006 Module Development Reference Manual

RoHS Compliance

JN5139 devices meet the requirements of Directive 2002/95/EC of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).

Status Information

The status of this Data Sheet is **Preliminary**.

Jennic products progress according to the following format:

Advance

The Data Sheet shows the specification of a product in planning or in development.

The functionality and electrical performance specifications are target values and may be used as a guide to the final specification. Integrated circuits are identified with an R suffix, for example JN5139-001R.

Jennic reserves the right to make changes to the product specification at anytime without notice.

Preliminary

The Data Sheet shows the specification of a product that is in production, but is not yet fully qualified.

The functionality of the product is final. The electrical performance specifications are target values and may used as a guide to the final specification. Integrated circuits are identified with an R# suffix, for example JN5139-001R1.

Jennic reserves the right to make changes to the product specification at anytime without notice.

Production

This is the final Data Sheet for the product; all product characterization is completed.

All functional and electrical performance specifications where included, including min and max values are final.

This Data Sheet supersedes all previous document versions.

Jennic reserves the right to make changes to the product specification at anytime.

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Version Control

Version	Notes
1.0	22rd December 2006 - First Release
1.1	9th February 2007 – Added solder reflow profile
1.2	16th July 2007 – uplifted to Preliminary status, typical specification updates, internal reset modifications
1.3	31st July 2007 – updates to DC current consumptions
1.4	26th October 2007 – updated applications information, added PCB decal including paddle details
1.5	23rd April 2008 – Internal only
1.6	26th September 2008 – added min/max specifications, incorporated known errata
1.7	3rd April 2009 – Datasheet fully revised
1.8	15th May 2009 – Tape and reel information revised

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