# Product Specification

(Preliminary)

**Part Name:** Monochrome LCD Display Module

**Part No.:** BGB12232-09 SERIES

**Doc No.:** SAS1-1330-A

| **Customer:** |
| --- |
| Approved by: |

| **From:** Blaze Display Technology Co., Ltd. |
| --- |
| Approved by: |


**Blaze Display Technology Co., Ltd.**

5/F, HSAE Tech Building, Hi-Tech Park, Nanshan, Shenzhen, China, 518057

Http://www.blazedisplay.com


**Notes:**

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2. The information contained herein is presented merely to indicate the characteristics and performance of our products. No responsibility is assumed by Blaze Display Technology Co., Ltd. for any intellectual property claims or other problems that may result application based on the module described herein.

## *Revised History*

| Part Number | Revision | Revision Content | Revised on |
|---|---|---|---|
| BGB12232-09-LW-FPTWD-1.0 | 1.0 | New | Aug. 30th, 2013 |

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# Contents



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# *1. Basic Specifications*

## 1.1 Display Specifications

| | |
|---|---|
| 1) Display Type: | FSTN, Blue / Negative |
| 2) Display Format: | 122×32 Dots White |
| 3) Graphic Color (ON): | Blue |
| 4) Background Color (ON): | Blue |
| Background Color (OFF): | 1/32Duty; 1/5Bias 6:00 |
| 5) Drive Method: | Transflective |
| 6) Viewing Direction: | |
| 7) Polarizer Type: | |

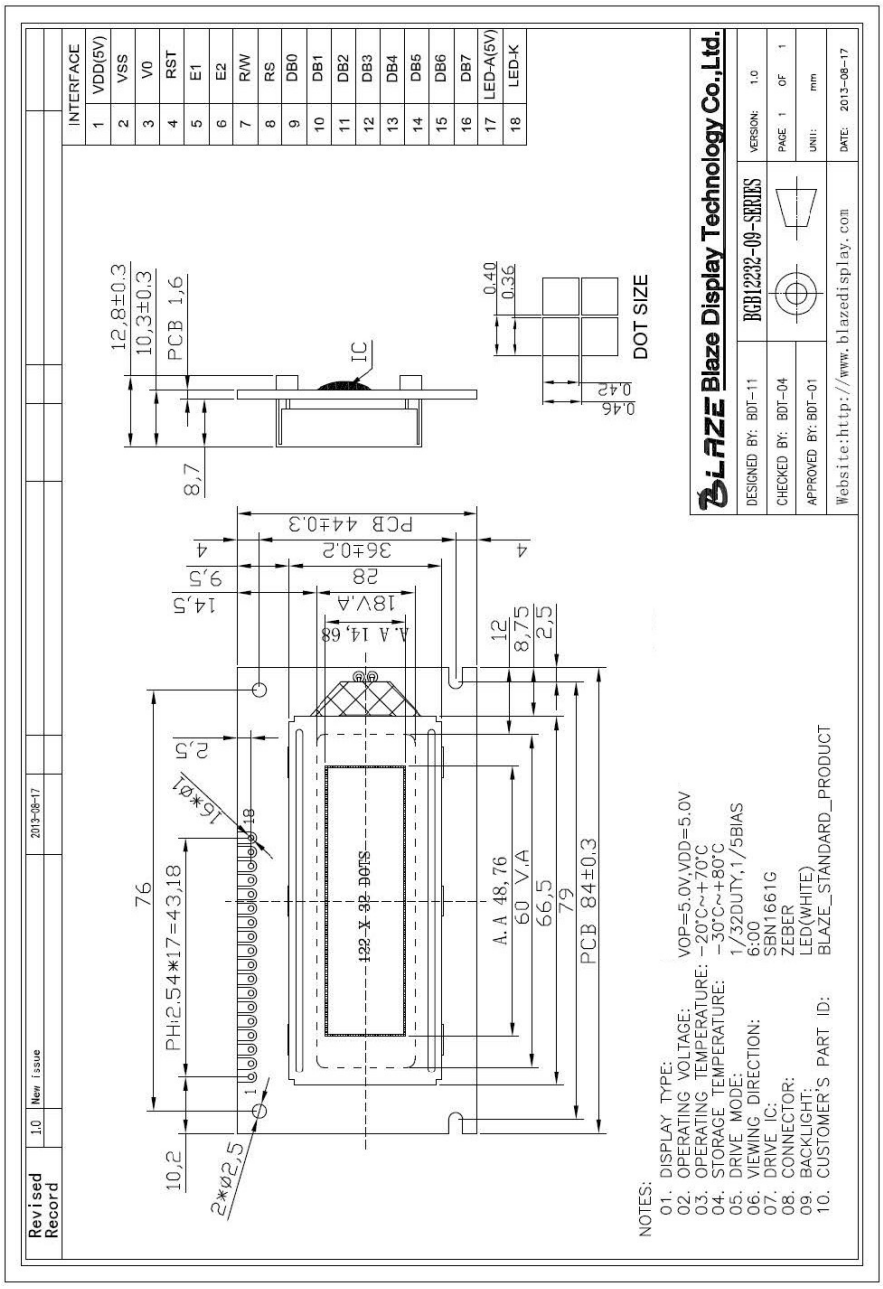
## 1.2 Mechanical Specifications

| | |
|---|---|
| 1) Outline Dimensions: | According to the annexed outline drawing on the next page |
| 2) Viewing Area: | 60.00 W × 18.00 H (mm) |
| 3) Active Area: | 48.76 W × 14.68 H (mm) |
| 4) Dot Pitch: | 0.40 W × 0.46H (mm) |
| 5) Dot Size: | 0.36W × 0.42H (mm) |
| 6) Weight: | T.B.D. |

## 1.3 Others

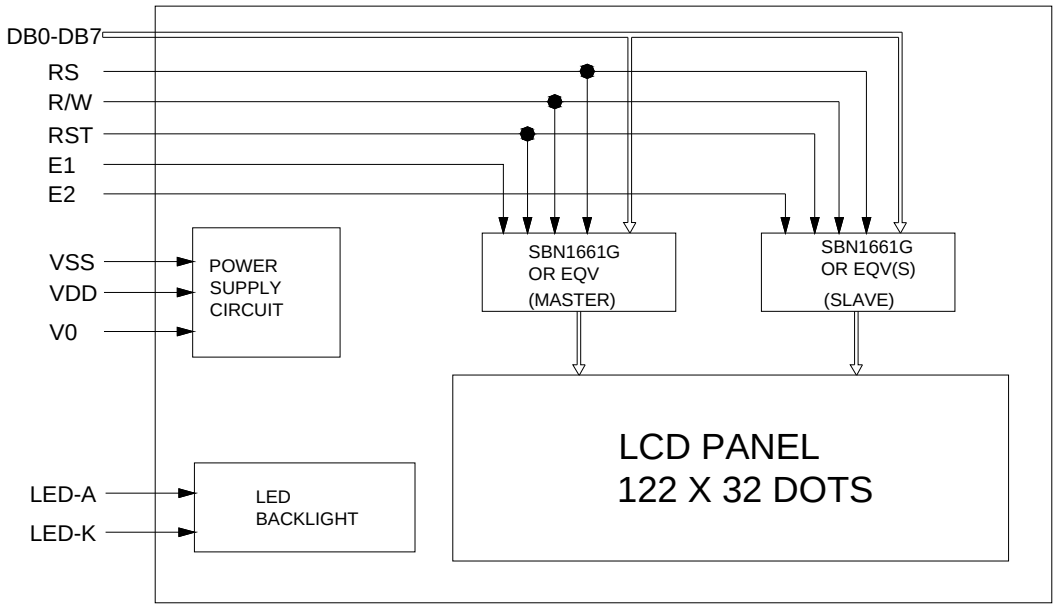
| | |
|---|---|
| 1) Driver IC: | SBN1661G or EQV |
| 2) Backlight: | LED, White, If =20mA, Vf = 5.0V |
| 3) Operating Temperature: | -20°C－ + 70°C |
| 4) Storage Temperature: | -30°C－ + 80°C |
| 5) RoHS Compliant: | Yes |

## 1.4 Mechanical Drawing



# 2. Electrical Specification

## 2.1 Block Diagram




## 2.2 Absolute Maximum Ratings

| Item | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| Power Supply for Logic | $V_{DD}$-$V_{SS}$ | −0.3 | — | +5.5 | V |
| Power supply for LCD Drive | $V_{DD}$-$V_0$ | −0.3 | — | 5.0 | V |
| Input Voltage | $V_I$ | $V_{SS}$ | — | $V_{DD}$ | V |
| Operating Temperature | $T_{OP}$ | −20 | — | +70 | °C |
| Storage Temperature | $T_{ST}$ | −30 | — | +80 | °C |
| Static Electricity | Be sure that you are grounded when handing LCM | | | | |

## 2.3 Electrical Characteristics

Ta = 25°C; Vdd = 4.5～5.0V, otherwise specified

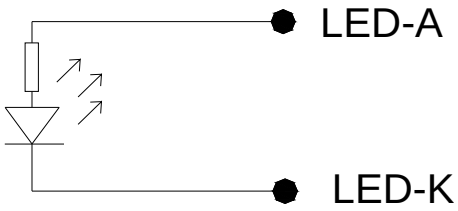
| Item | Symbol | Standard Value | | | Test Condition | Unit |
|---|---|---|---|---|---|---|
| | | Min. | Typ. | Max. | | |
| Supply Current for Logic | $V_{DD}$ | +4.8 | +5.0 | +5.2 | — | V |
| Supply Current for Logic | $I_{DD}$ | — | TBD | — | — | mA |
| Supply Current for LCD | $V_{LCD}$ | +4.6 | +4.8 | +5.0 | 25 | °C |

### 2.4 Pin Definition

| Pin No. | Symbol | Level | Description |
|---|---|---|---|
| 1 | VDD | - | Power supply |
| 2 | VSS | - | System ground |
| 3 | V0 | - | Contrast adjust |
| 4 | RST | - | System resets signal |
| 5 | E1 | - | Write or Read enable signal(Master) |
| 6 | E2 | - | Write or Read enable signal(Slave) |
| 7 | R/W | - | Read or Write select signal |
| 8 | RS | - | Data/Instruction select |
| 9 | DB0 | H/L | Data bit 0 |
| 10 | DB1 | H/L | Data bit 1 |
| 11 | DB2 | H/L | Data bit 2 |
| 12 | DB3 | H/L | Data bit 3 |
| 13 | DB4 | H/L | Data bit 4 |
| 14 | DB5 | H/L | Data bit 5 |
| 15 | DB6 | H/L | Data bit 6 |
| 16 | DB7 | H/L | Data bit 7 |
| 17 | LED-A | - | LED light anode (+5V) |
| 18 | LED-K | - | LED light cathode |

## *3. LED Backlight*

### 3.1 Power Supply for LED Backlight



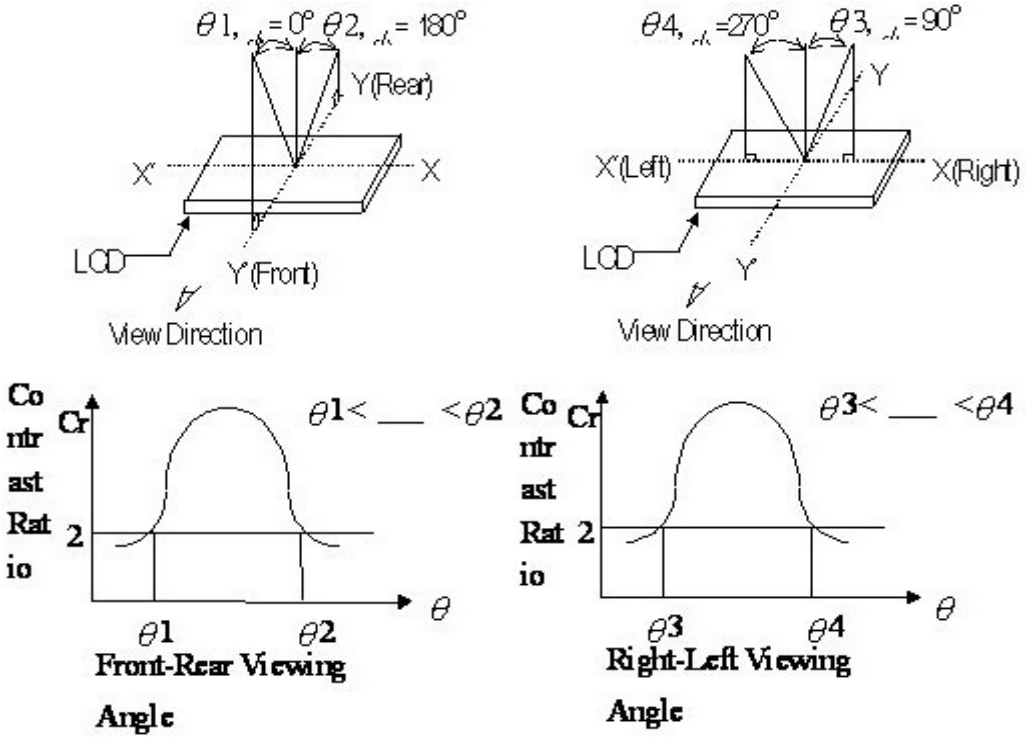

### 3.2 Electrical Optical Characteristics

Ta = 25°C; Vdd = 4.5～5.0V, otherwise specified

| Item | Symbol | Conditions | Standard Value | | | Unit |
|---|---|---|---|---|---|---|
| | | | Min. | Typ. | Max. | |
| Forward Voltage | Vf | If = 20mA | 4.8 | 5.0 | 5.2 | V |
| Reverse Current | Ir | Vr = 5V | – | – | 100 | uA |
| Spectral Line Half Width | △λ | IF =20mA | – | – | – | nm |
| Peak Wave Length | λp | T = 25℃ | – | – | – | nm |
| Luminance | Lv | IF = 20mA | 35 | - | – | cd/m$^2$ |
| Uniformity | △ | Min / Max = 100% | 70% | – | - | % |

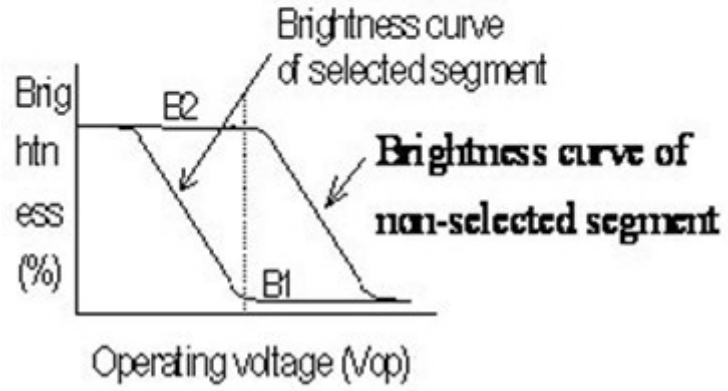
# *4. Optical Characteristics*

## 4.1 Definition of Viewing Angle

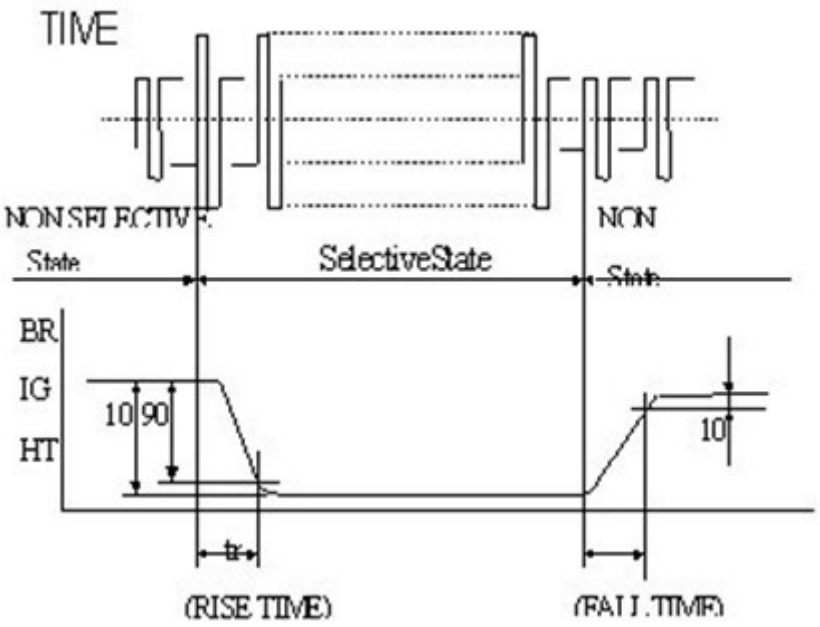



## 4.2 Definition of Contrast

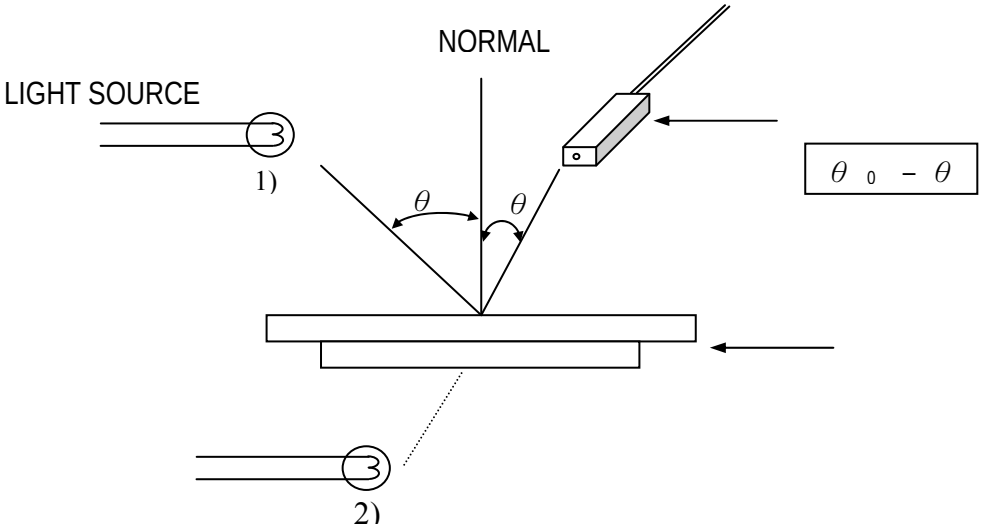
$$C.R = \frac{\text{Brightness of nonselected segment (B2)}}{\text{Brightness of selected segment}} \quad \text{RATIO}$$



### 4.3 Definition of Response




### 4.4 Measuring Instruments For Electro-optical Characteristics




*** Note:**

1) Light source position for measuring the reflective type of LCD panel;
2) Light source position for measuring the transflective / transmissive types of LCD panel.

# 5. Timing Diagrams

## 5.1 Interface Timing

### 14.2 AC timing for interface with an 80-type microcontroller

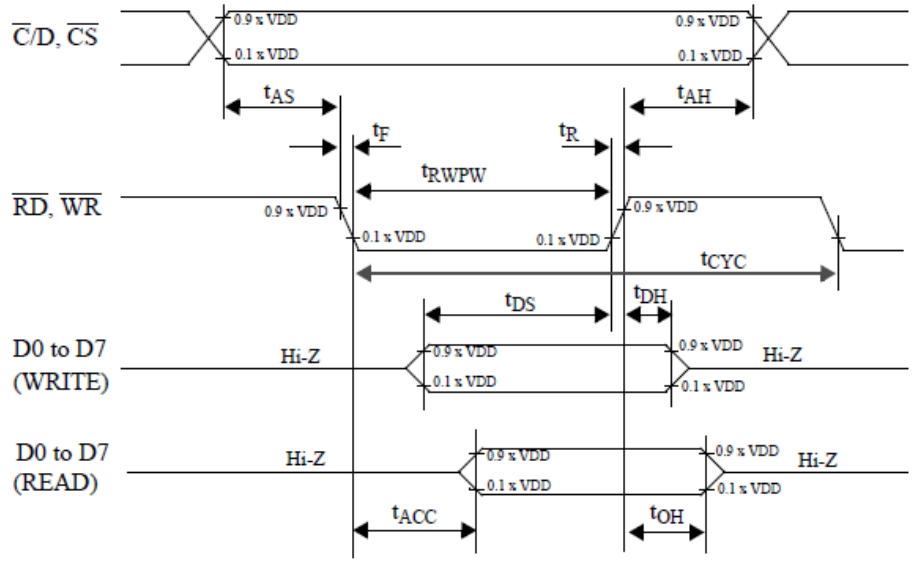



Fig.22 AC timing for interface with a 80-type microcontroller

**Table 42** AC timing for interface with a 80-type microcontorller at $V_{DD}$=5 volts

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS}$ | Address set-up time | 20 | | | ns |
| $t_{AH}$ | Address hold time | 10 | | | ns |
| $t_F$, $t_R$ | Read/Write pulse falling/rising time | | 15 | | ns |
| $t_{RWPW}$ | Read/Write pulse width | 200 | | | ns |
| $t_{CYC}$ | System cycle time | 1000 | | | ns |
| $t_{DS}$ | Data setup time | 80 | | | ns |
| $t_{DH}$ | Data hold time | 10 | | | ns |
| $t_{ACC}$ | Data READ access time | | 90 | CL= 100 pF. | ns |
| $t_{OH}$ | Data READ output hold time | 10 | 60 | Refer to Fig. 23. | ns |

**Table 43** AC timing for interface with an 80-type microcontorller at $V_{DD}$=3 volts

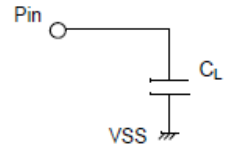
$V_{DD}$ = 3 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS}$ | Address set-up time | 40 | | | ns |
| $t_{AH}$ | Address hold time | 20 | | | ns |
| $t_F$, $t_R$ | Read/Write pulse falling/rising time | | 15 | | ns |
| $t_{RWPW}$ | Read/Write pulse width | 400 | | | ns |
| $t_{CYC}$ | System cycle time | 2000 | | | ns |
| $t_{DS}$ | Data setup time | 160 | | | ns |

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{DH}$ | Data hold time | 20 | | | ns |
| $t_{ACC}$ | Data READ access time | | 180 | CL= 100 pF, | ns |
| $t_{OH}$ | Data READ output hold time | 20 | 120 | Refer to 23. | ns |

**Note:**

The measurement is with the load circuit connected. The load circuit is shown in Fig. 23.




$C_L$= 100 pF (including wiring and probe capacitance).

Fig.23 Load circuit.

### 14.3 AC timing for interface with a 68-type microcontroller

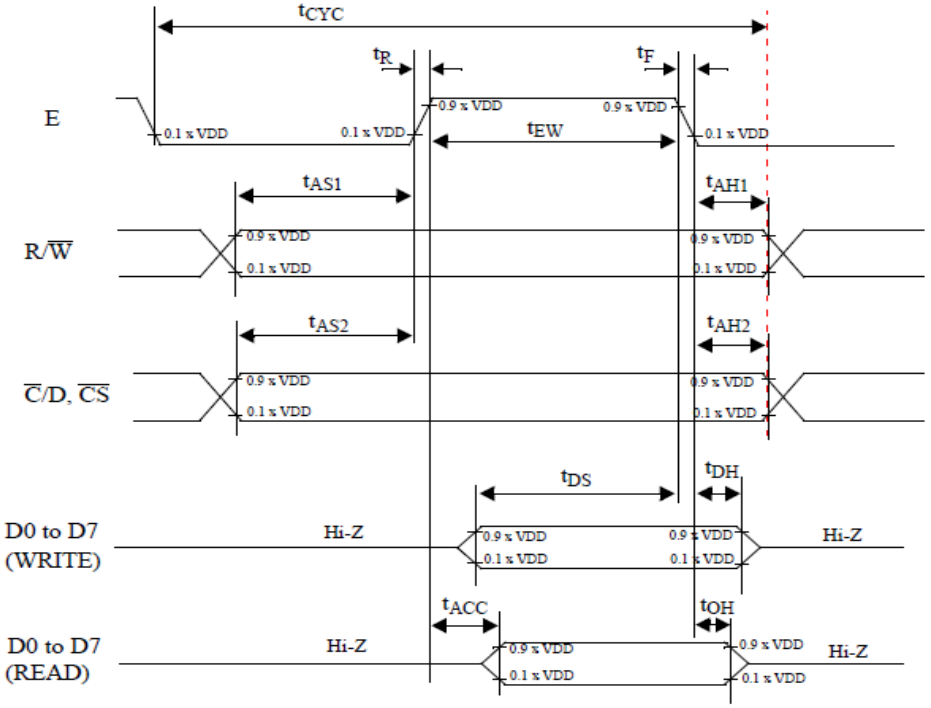



Fig.24 AC timing for interface with a 68-type microcontroller

**Table 44** AC timing for interface with a 68-type microcontroller at $V_{DD}$=5 volts

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS1}$ | Address set-up time with respect to R/$\overline{W}$ | 20 | | | ns |
| $t_{AS2}$ | Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$ | 20 | | | ns |
| $t_{AH1}$ | Address hold time with respect to R/$\overline{W}$ | 10 | | | ns |
| $t_{AH2}$ | Address hold time respect with to $\overline{C}$/D, $\overline{CS}$ | 10 | | | ns |
| $t_F$, $t_R$ | Enable (E) pulse falling/rising time | | 15 | | ns |
| $t_{CYC}$ | System cycle time | 1000 | | Note 1 | ns |
| $t_{EWR}$ | Enable pulse width for READ | 100 | | | ns |
| $t_{EWW}$ | Enable pulse width for WRITE | 80 | | | ns |
| $t_{DS}$ | Data setup time | 80 | | | ns |
| $t_{DH}$ | Data hold time | 10 | | | ns |
| $t_{ACC}$ | Data access time | | 90 | CL= 100 pF. | ns |
| $t_{OH}$ | Data output hold time | 10 | 60 | Refer to Fig. 23. | ns |

**Table 45** AC timing for interface with a 68-type microcontroller at $V_{DD}$=3 volts

$V_{DD}$ = 3 V ±10%; $V_{SS}$ = 0 V; $T_{amb}$ = -20 °C to +75°C.

| symbol | parameter | min. | max. | test conditons | unit |
|---|---|---|---|---|---|
| $t_{AS1}$ | Address set-up time with respect to R/$\overline{W}$ | 40 | | | ns |
| $t_{AS2}$ | Address set-up time with respect to $\overline{C}$/D, $\overline{CS}$ | 40 | | | ns |
| $t_{AH1}$ | Address hold time with respect to R/$\overline{W}$ | 20 | | | ns |
| $t_{AH2}$ | Address hold time respect with to $\overline{C}$/D, $\overline{CS}$ | 20 | | | ns |
| $t_F$, $t_R$ | Enable (E) pulse falling/rising time | | 15 | | ns |
| $t_{CYC}$ | System cycle time | 2000 | | Note 1 | ns |
| $t_{EWR}$ | Enable pulse width for READ | 200 | | | ns |
| $t_{EWW}$ | Enable pulse width for WRITE | 160 | | | ns |
| $t_{DS}$ | Data setup time | 160 | | | ns |
| $t_{DH}$ | Data hold time | 20 | | | ns |
| $t_{ACC}$ | Data access time | | 180 | CL= 100 pF. | ns |
| $t_{OH}$ | Data output hold time | 20 | 120 | Refer to Fig. 23. | ns |

**Note:**

1. The system cycle time($t_{CYC}$) is the time duration from the time when Chip Enable is enabled to the time when Chip Select is released.

## 5.2 DC Characteristics

**Table 39** DC Characteristics

$V_{DD}$ = 5 V ±10%; $V_{SS}$ = 0 V; all voltages with respect to $V_{SS}$, unless otherwise specified; $T_{amb}$ = –20 to +75 °C.

| SYMBOL | PARAMETER | CONDITIONS | MIN. | TYP. | MAX. | UNIT |
|---|---|---|---|---|---|---|
| $V_{DD}$ | Supply voltage for logic | | 4.5 | 5.0 | 5.5 | V |
| $V_{LCD}$ | LCD bias voltage $V_{LCD}$= $V_{DD}$-V5 | | | | 13 | V |
| $V_{IL}$ | LOW level input voltage | For all inputs | 0 | | 0.8 | V |
| $V_{IH}$ | HIGH level input voltage | For all inputs | $V_{DD}$-1.2 | | $V_{DD}$ | V |
| $V_{OL}$ | LOW level output voltage | For all outputs | 0.0 | | 0.3 | V |
| $V_{OH}$ | HIGH level output voltage | For all outputs | $V_{DD}$ - 0.3 | | $V_{DD}$ | V |
| $I_{STBY}$ | Standby current at $V_5$=-5 volts | Note 1 | | | 3.0 | µA |
| $I_{DD(1)}$ | Operating current at $V_5$=-5 volts and $f_{CL}$=2KHz, $V_{LCD}$=10 volts | Note 2 & Note 3 | | 2.7 | 5.6 | µA |
| $I_{DD(2)}$ | Operating current at $V_5$=-5 volts and Rf=1 MΩ, $V_{LCD}$=10 volts | | | 12.3 | 15.6 | µA |
| $I_{DD(3)}$ | Operating current at $V_5$=-5 volts and $f_{CL}$=21.8 KHz, $V_{LCD}$=10 volts | | | 5.3 | 10.8 | µA |
| $I_{DD(4)}$ | Operating current at $V_5$=-5 volts and $t_{CYC}$=100 KHz, $V_{LCD}$=10 volts | Note 4 | | 21.7 | 26.2 | µA |
| $f_{osc(VDD=5V)}$, $f_{osc(VDD=3V)}$ | Please refer to Table 37, On-chip RC oscillator characteristics. | | | | | |
| $C_{in}$ | Input capacitance of all input pins | | | 5.0 | 8.0 | pF |
| $R_{ON}$ | LCD driver ON resistance | Note 5 | | 5.0 | 7.5 | KΩ |
| $t_R$ | Reset time | Note 6 | 1.0 | | | µS |

**Notes:**

1. Conditions for the measurement: OSC1=OSC2=VDD, measured at the $V_{DD}$ pin.
2. These values are measured when the microcontroller does not perform any READ/WRITE operation to the chip.
3. These meaurements are for different members of the series:
   a) $I_{DD(1)}$ are measured for the SBN1661G_M02 and the SBN0080G_S02,
   b) $I_{DD(2)}$ are measured for the SBN1661G_M18, and
   c) $I_{DD(3)}$ are measured for the SBN0080G_S18.
4. These values are measured when the microcontroller continuously performs READ/WRITE operation to the chip.
5. This measurement is for the transmission high-voltage PMOS or NMOS of COM0~15 and SEG0~60(79). Please refer to Section 18 for these driver circuit. The meaurement is for the case when the voltage differential between the source and the drain of the high voltage PMOS or NMOS is 0.1 volts.
6. The value is relative to the RESET pulse edge. That is, 1.0 µS after the last RESET edge, the device is completely reset.

## 5.3 External reset Timing

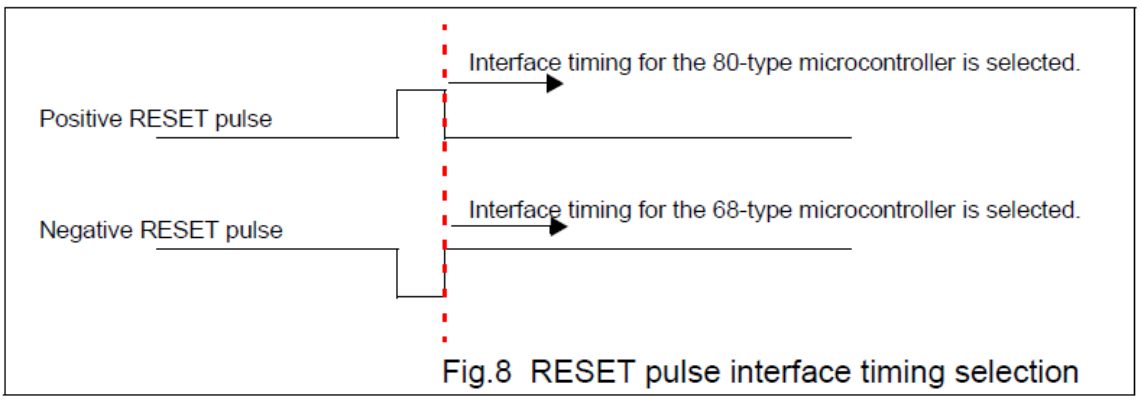



Fig.8 RESET pulse interface timing selection

## 6. Instruction Table

Table 3 Commands

| | Command | Code | | | | | | | | | | Function | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | | A0 | $\overline{RD}$ | $\overline{WR}$ | D7 | D6 | D5 | D4 | D3 | D2 | D1 | D0 | |
| (1) | Display ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0/1 | Turns all display on or off, independently of display RAM data or internal status.<br>1: ON<br>0: OFF (Power-saving mode with static drive on)* | |
| (2) | Display start line | 0 | 1 | 0 | 1 | 1 | 0 | Display Start Address (0–31) | | | | | Specifies RAM line corresponding to uppermost line (COM0) of display. | |
| (3) | Set page address | 0 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 0 | Page (0–3) | | Sets display RAM page in page address register. | |
| (4) | Set column (segment) address | 0 | 1 | 0 | 0 | Column Address (0–79) | | | | | | | Sets display RAM column address in column address register. | |
| (5) | Read status | 0 | 0 | 1 | Busy | ADC | ON/OFF | RESET | 0 | 0 | 0 | 0 | Reads the following status:<br>BUSY 1: Internal operation, 0: Ready<br>ADC 1: CW output (forward), 0: CCW output (reverse)<br>ON/OFF 1: Display off, 0: Display on<br>RESET 1: Being reset, 0: Normal | |
| (6) | Write display data | 1 | 1 | 0 | Write Data | | | | | | | | Writes data from data bus into display RAM. | Display RAM location whose address has been preset is accessed. After access, the column address is incremented by 1. |
| (7) | Read display data | 1 | 0 | 1 | Read Data | | | | | | | | Reads data from display RAM onto data bus. | |
| (8) | Select ADC | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | 0/1 | Used to invert relationship of assignment between display RAM column addresses and segment driver outputs.<br>0: CW output (forward)<br>1: CCW output (reverse) | |
| (9) | Static drive ON/OFF | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 0/1 | Selects normal display or static driving operation.<br>1: Static drive (power-saving mode)<br>0: Normal driving | |
| (10) | Select duty | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 1 | 0 | 0 | 0/1 | Selects LCD cell driving duty.<br>1: 1/32<br>0: 1/16 | |
| (11) | Read modify write | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | Increments column address counter by 1 when display data is written. (This is not done when data is read.) | |
| (12) | End | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 1 | 1 | 1 | 0 | Clears read modify write mode. | |
| (13) | Reset | 0 | 1 | 0 | 1 | 1 | 1 | 0 | 0 | 0 | 1 | 0 | Sets display start line register on the first line. Also sets column address counter and page address counter to 0. | |

* With display off (command (1)), static drive going on (9) invokes power-saving mode.

# 7. Reliability Specification

## 7.1 Contents of Reliability Tests

| No. | Test Item | Content of Test | Test Condition |
|---|---|---|---|
| 1 | High Temperature Storage | Endurance test applying the high storage temperature for a long time | +80°C<br>96H |
| 2 | Low Temperature Storage | Endurance test applying the low storage temperature for a long time | −30°C<br>96H |
| 3 | High Temperature Operation | Endurance test applying the electric stress (voltage & current) and the thermal stress to the element for a long time | +70°C<br>96H |
| 4 | Low Temperature Operation | Endurance test applying the electric stress under low temperature for a long time | −20°C<br>96H |
| 5 | High Temperature/ Humidity Storage | Endurance test applying the high temperature and humidity storage for a long time | 40°C<br>90%RH<br>96H |
| 6 | Temperature Cycle | Endurance test applying the low and high temperature cycle<br>−20°C ⟷ 25°C ⟷ 70°C ⟷ 25°C<br>30min 5min 30min 5min<br>⟷<br>1 cycle | −20°C/70°C<br>10 cycles |
| 7 | Vibration Test (Package State) | Endurance test applying the vibration during transportation | 10Hz－55Hz,<br>50m/s, 15min |
| 8 | Shock Test (Package State) | Endurance test applying the shock during transportation | Half-sinewave,<br>100m/s, 11ms |
| 9 | Atmospheric Pressure Test | Endurance test applying the atmospheric pressure during transportation by air | 40 kPa<br>16 H |

## 7.2 Life Time

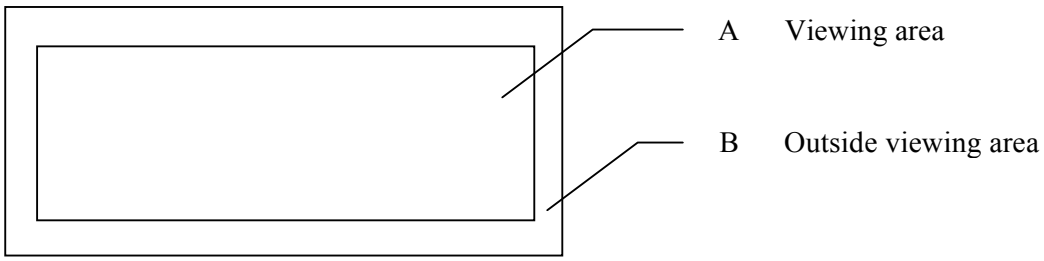
| Item | Description |
|---|---|
| 1 | Function, performance, appearance, etc. shall be free from remarkable deterioration within 50,000 hours under ordinary operating and storage conditions of room temperature (25±10°C), normal humidity (45±20% RH), and in area not exposed to direct sunlight. |

*** Note: Test Condition**

1) Temperature and humidity: If no specification, Temperature set at 25±2°C, Humidity set at 60±5%RH;
2) Operating state: Samples subject to the tests shall be in " Operating " condition.

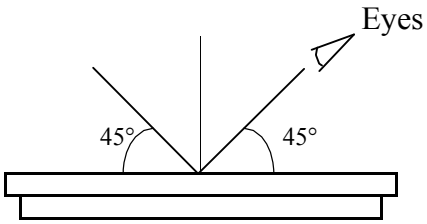
# 8. Quality Level

## 8.1 Zone Definition



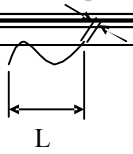

## 8.2 Visual Inspection

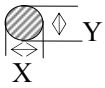
1) Inspect under 2x20W or 40W fluorescent lamp (approximately 3000 lux) leaving 25 to 30 cm between the module and the lamp and 30 cm between the module and the eye (measuring position).
2) Appearance is inspected at the best contrast voltage (best contrast is adjusted considering clearness and crosstalk on screen).
3) Inspect the module at 45° right and left, top and bottom.
4) Use the optimum viewing angle during the contrast inspection.

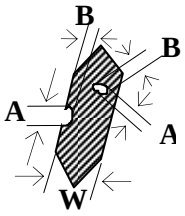


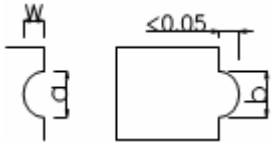

## 8.3 Standard of Apperance Inspection

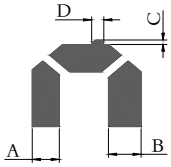
<table>
<tr><th>No.</th><th>Item</th><th>Criteria</th></tr>
<tr><td>1</td><td>Black spot<br>White spot<br>Dust</td><td>Round type: as per following drawing<br>Φ = (X+Y)/2<br>  <br>X<br><table><tr><td colspan="3">Acceptable quantity</td></tr><tr><td>Size</td><td>Zone A</td><td>Zone B</td></tr><tr><td>Φ <0.1</td><td>Any number</td><td rowspan="4">Any number</td></tr><tr><td>0.1< Φ <0.2</td><td>2</td></tr><tr><td>0.2< Φ <0.25</td><td>1</td></tr><tr><td>0.25< Φ</td><td>0</td></tr></table><br>Line type: as per following drawing<br>W</td></tr>
</table>

<table>
<tr><td></td><td></td><td>


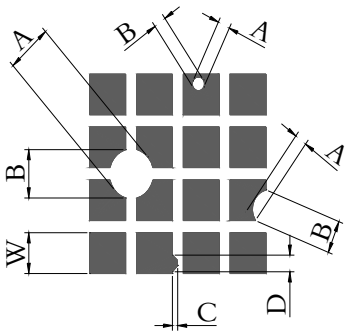
<table>
<tr><th colspan="4">Acceptable quantity</th></tr>
<tr><th>Length</th><th>Width</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>—</td><td>W≤0.02</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>L≤3.0</td><td>0.02<W≤0.03</td><td rowspan="2">2</td></tr>
<tr><td>L≤2.5</td><td>0.03<W≤0.05</td></tr>
<tr><td>—</td><td>0.05<W</td><td>As round type</td></tr>
</table>
Total<br>acceptable quantity: 3
</td></tr>
<tr><td>2</td><td>Polariser scratch</td><td>Scratch on protective film is permitted<br>Scratch on polariser: same as No. 1</td></tr>
<tr><td>3</td><td>Polariser bubble</td><td>Φ = (X+Y)/2<br>


<table>
<tr><th colspan="3">Acceptable quantity</th></tr>
<tr><th>Size</th><th>Zone A</th><th>Zone B</th></tr>
<tr><td>Φ <0.2</td><td>Any number</td><td rowspan="4">Any number</td></tr>
<tr><td>0.2< Φ <0.5</td><td>2</td></tr>
<tr><td>0.5< Φ <1.0</td><td>1</td></tr>
<tr><td>1.0< Φ</td><td>0</td></tr>
</table>
Total acceptable quantity: 3</td></tr>
<tr><td>4</td><td>Segment deformation</td><td>4.1 Pin hole on segmented display<br>W: segment width<br>Φ = (A+B)/2<br>


<table>
<tr><th colspan="2">Acceptable quantity</th></tr>
<tr><th>Width</th><th>Quantity</th></tr>
<tr><td>W≤0.4</td><td>Φ ≤0.2 and Φ ≤1/2W</td></tr>
<tr><td>W>0.4</td><td>Φ ≤0.25 and<br>Φ ≤1/3W</td></tr>
<tr><td colspan="2">Total acceptable quantity: 1 defect per segment<br>Pin holes with Φ under 0.10 mm are acceptable</td></tr>
</table>
4.2 Pin hole on dot matrix display<br>


<table>
<tr><th colspan="2">Acceptable quantity</th></tr>
<tr><th>Size</th><th></th></tr>
<tr><td>a, b<0.1</td><td>Any number</td></tr>
<tr><td>(a+b)/2≤0.1</td><td>Any number</td></tr>
<tr><td>0.5< Φ <1.0</td><td>3</td></tr>
</table>
Total acceptable quantity: 7<br><br>4.3 Segments / dots with different width<br>


<table>
<tr><th colspan="2">Acceptable</th></tr>
<tr><td>a≥b</td><td>a/b≤4/3</td></tr>
<tr><td>a<b</td><td>a/b>4/3</td></tr>
</table>
4.4 Alignment layer defect<br>Φ = (A+B)/2</td></tr>
</table>

<table>
<tr><td></td><td></td><td>


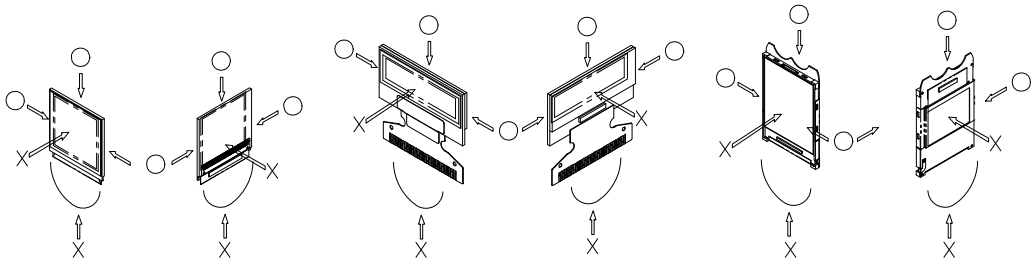
<table>
<tr><td colspan="2">Acceptable quantity</td></tr>
<tr><td>Size</td><td></td></tr>
<tr><td>Φ ≤0.4</td><td>Any number</td></tr>
<tr><td>0.4< Φ ≤1.0</td><td>5</td></tr>
<tr><td>1.0< Φ ≤1.5</td><td>3</td></tr>
<tr><td>1.5< Φ ≤2.0</td><td>2</td></tr>
</table>
Total acceptable quantity: 7
</td></tr>
<tr><td>5</td><td>Colour uniformity</td><td>Level of sample for approval set as limit sample</td></tr>
<tr><td>6</td><td>Backlight</td><td>The backlight colour should correspond to the product specification<br>Flashing and or unlit backlight is not allowed<br>Dust larger than 0.25 mm is not allowed</td></tr>
<tr><td>7</td><td>COB</td><td>Exposed wire bond pad is not allowed<br>Insufficient covering with resin is not allowed (wire bond line exposed) Dust or bubble on the resin are not allowed</td></tr>
<tr><td>8</td><td>PCB</td><td>No unmelted solder paste should be present on PCB<br>Cold solder joints, missing solder connections, or oxidation are not allowed<br>No residue or solder balls on PCB are allowed<br>Short circuits on components are not allowed</td></tr>
<tr><td>9</td><td>Tray particles</td><td>
<table>
<tr><td colspan="3">Acceptable quantity</td></tr>
<tr><td></td><td>Size</td><td>Quantity</td></tr>
<tr><td rowspan="2">On tray</td><td>Φ <0.2</td><td>Any number</td></tr>
<tr><td>Φ >0.25</td><td>4</td></tr>
<tr><td rowspan="2">On display</td><td>Φ ≥0.25</td><td>2</td></tr>
<tr><td>L = 3</td><td>1</td></tr>
</table>
</td></tr>
</table>

## *9. Percautions When Using These LCD Modules*

### 9.1 Handling Precautions

1) Since the display panel is being made of glass, do not apply mechanical impacts such us dropping from a high position.
2) If the display panel is broken by some accident and the internal organic substance leaks out, be careful not to inhale nor lick the organic substance.

3) If pressure is applied to the display surface or its neighborhood of the LCD Module, the cell structure may be damaged and be careful not to apply pressure to these sections.
4) The polarizer covering the surface of the LCD Module is soft and easily scratched. Please be careful when handling the LCD Module.
5) When the surface of the polarizer of the LCD Module has soil, clean the surface. It takes dvantage of by using following adhesion tape.
   * Scotch Mending Tape No. 810 or an equivalent.
   Never try to breathe upon the soiled surface nor wipe the surface using cloth containing solvent such as ethyl alcohol, since the surface of the polarizer will become cloudy.
   Also, pay attention that the following liquid and solvent may spoil the polarizer:
   * Water
   * Ketone
   * Aromatic Solvents
6) Hold LCD Module very carefully when palcing LCD Module into the system housing. Do not apply excessive stress or pressure to LCD Module. And, do not over bend the film with electrode pattern layouts. These stresses will influence the display performance. Also, secure sufficient rigidity for the outer cases.



7) Do not apply stress to the LSI chips and the surrounding molded sections.
8) Do not disassemble nor modify the LCD Module.
9) Do not apply input signals while the logic power is off.
10) Pay sufficient attention to the working environments when handing LCD Modules to prevent occurrence of element breakage accidents by static electricity.
    * Be sure to make human body grounding when handling LCD Modules.
    * Be sure to ground tools to use or assembly such as soldering irons.
    * To suppress generation of static electricity, avoid carrying out assembly work under dry environments.
    * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film.
    * Protective film is being applied to the surface of the display panel of the LCD Module. Be careful since static electricity may be generated when exfoliating the protective film
11) Protection film is being applied to the surface of the display panel and removes the protection film before assembling it. At this time, if the LCD Module has been stored for a long period of time, residue adhesive material of the protection film may remain on the surface of the display panel after removed of the film. In such case, remove the residue material by the method introduced in the above Section 5).
12) If electric current is applied when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful to avoid the above.

### 9.2 Storage Precautions

1) When storing LCD Modules, put them in static electricity preventive bags avoiding exposure to direct sun light nor to lights of fluorescent lamps. and, also, avoiding high temperature and high humidity environment or low temperature (less than 0°C) environments. (We recommend you to store these modules in the packaged state when they were shipped from Blaze Display Technology Co., Ltd.)
   At that time, be careful not to let water drops adhere to the packages or bags nor let dewing occur with them.
2) If electric current is applied when water drops are adhering to the surface of the LCD Module, when the LCD Module is being dewed or when it is placed under high humidity environments, the electrodes may be corroded and be careful about the above.

### 9.3 Designing Precautions

1) The absolute maximum ratings are the ratings which can not be exceeded for LCD Module, and if these values are exceeded, panel damage may be happen.
2) To prevent occurrence of malfunctioning by noise, pay attention to satisfy the VIL and VIH specifications and, at the same time, to make the signal line cable as short as possible.
3) We recommend you to install excess current preventive unit (fuses, etc.) to the power circuit (VDD). (Recommend value: 0.5A)
5) Pay sufficient attention to avoid occurrence of mutual noise interference with the neighboring devices.
6) As for EMI, take necessary measures on the equipment side basically.
   When fastening the LCD Module, fasten the external plastic housing section.
7) If power supply to the LCD Module is forcibly shut down by such errors as taking out the main battery while the LCD Panel is in operation, we cannot guarantee the quality of this LCD Module.
8) The electric potential to be connected to the rear face of the IC chip should be as follows:
   * Connection (contact) to any other potential than the above may lead to rupture of the IC.

### 9.4 Precautions When Disposing of the LCD Modules

Request the qualified companies to handle industrial wastes when disposing of the LCD Modules. Or, when burning them, be sure to observe the environmental and hygienic laws and regulations.

### 9.5 Other Precautions

1) When a LCD Module is operated for a long of time with fixed pattern may remain as an after image or slight contrast deviation may occur.
   Nonetheless, if the operation is interrupted and left unused for a while, normal state can be restored. Also, there will be no problem in the reliability of the module
2) To protect LCD Modules from performance drops by static electricity rapture, etc., do not touch the following sections whenever possible while handling the LCD Modules.

* Pins and electrodes
* Pattern layouts such as the TCP & FPC

3) With this LCD Module, the LCD Module driver is being exposed. Generally speaking, semiconductor elements change their characteristics when light is radiated according to the principle of the solar battery. Consequently, if this LCD Module driver is exposed to light, malfunctioning may occur.
   * Design the product and installation method so that the LCD Module driver may be shielded from light in actual usage.
   * Design the product and installation method so that the LCD Module driver may be shielded from light during the inspection processes.
4) Although this LCD Module stores the operation state data by the commands and the indication data, when excessive external noise, etc. enters into the module, the internal status may be changed to take appropriate measures to suppress noise generation or to protect from influences of noise on the system design.
5) We recommend you to construct its software to make periodical refreshment of the operation statuses (re-setting of the commands and re-transference of the display data) to cope with catastrophic noise.