Future Technology Devices International Ltd.

UM245R USB-Parallel FIFO Development Module

Incorporating FTDIChip-ID™ Security Dongle

The **UM245R** *is a development module which uses FTDI's FT245RL, the latest device to be added to FTDI's range of USB UART interface Integrated Circuit Devices.*

The FT245R is a USB to parallel FIFO interface, with the new FTDIChip-ID™ security dongle feature. In addition, asynchronous and synchronous bit bang interface modes are available. USB to parallel designs using the FT245R have been further simplified by fully integrating the external EEPROM, clock circuit and USB resistors onto the device.

The FT245R adds a new function compared with its predecessors, effectively making it a "2-in-1" chip for some application areas. A unique number (the FTDIChip-ID™) is burnt into the device during manufacture and is readable over USB, thus forming the basis of a security dongle which can be used to protect customer application software from being copied.

The UM245R is supplied on a PCB which is designed to fit a 24 pin DIP socket. All components used, including the FT232RL are Pb-free (RoHS compliant).

1. Features

1.1 Hardware Features

- Single chip USB to parallel FIFO bidirectional data transfer interface.
- Entire USB protocol handled on the chip - No USB-specific firmware programming required.
- Simple interface to MCU / PLD / FPGA logic with simple 4-wire handshake interface.
- Data transfer rate to 1 Megabyte / second - D2XX Direct Drivers.
- Data transfer rate to 300 kilobyte / second - VCP Drivers.
- FTDI's royalty-free VCP and D2XX drivers eliminate the requirement for USB driver development in most cases.
- New USB FTDIChip-ID™ feature.
- FIFO receive and transmit buffers for high data throughput.
- Adjustable receive buffer timeout.
- Synchronous and asynchronous bit bang mode interface options with RD# and WR# strobes allow the data bus to be used as a general purpose I/O port.
- Integrated 1024 Byte internal EEPROM for storing USB VID, PID, serial number and product description strings.
- Device supplied preprogrammed with unique USB serial number.
- Support for USB suspend / resume through PWREN# pin and Wake Up pin function.
- In-built support for event characters.
- Support for bus powered, self powered, and high-power bus powered USB configurations.
- Integrated 3.3V level converter for USB I/O .
- Integrated level converter on FIFO interface and control pins for interfacing to 5V - 1.8V Logic.
- True 5V / 3.3V / 2.8V / 1.8V CMOS drive output and TTL input.
- High I/O pin output drive option.
- Integrated USB resistors.
- Integrated power-on-reset circuit.
- Fully integrated clock - no external crystal, oscillator, or resonator required.
- Fully integrated AVCC supply filtering - No separate AVCC pin and no external R-C filter required.
- USB bulk transfer mode.
- 3.3V to 5.25V Single Supply Operation.
- Low operating and USB suspend current.
- Low USB bandwidth consumption.
- UHCI / OHCI / EHCI host controller compatible
- USB 2.0 Full Speed compatible.
- -40°C to 85°C extended operating temperature range.
- Available in compact Pb-free 28 Pin SSOP and QFN-32 packages (both RoHS compliant).
- Supplied in PCB designed to fit 24 pin DIP socket
- Connect to a PC via a standard USB A to B USB cable.

1.2 Driver Support

Royalty-Free VIRTUAL COM PORT (VCP) DRIVERS for...

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- MAC OS 8 / 9, OS-X
- Linux 2.4 and greater

Royalty-Free D2XX *Direct* Drivers (USB Drivers + DLL S/W Interface)

- Windows 98, 98SE, ME, 2000, Server 2003, XP.
- Windows Vista / Longhorn*
- Windows XP 64-bit.*
- Windows XP Embedded.
- Windows CE.NET 4.2 & 5.0
- Linux 2.4 and greater

The drivers listed above are all available to download for free from the FTDI website. Various 3rd Party Drivers are also available for various other operating systems - see the FTDI website for details.

* Currently Under Development. Contact FTDI for availability.

1.3 Typical Applications

- Upgrading Legacy Peripherals to USB
- Cellular and Cordless Phone USB data transfer cables and interfaces
- Interfacing MCU / PLD / FPGA based designs to USB
- USB Audio and Low Bandwidth Video data transfer
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Hardware Modems
- USB Wireless Modems
- USB Bar Code Readers
- USB Software / Hardware Encryption Dongles

2. Features and Enhancements

2.1 Key Features

This section summarises the key features and enhancements of the FT245R IC device which is used in the UM245R Module. For further details, consult the FT245R datasheet, which is available from the FTDI website.

Integrated Clock Circuit - Previous generations of FTDI's USB to parallel FIFO interface devices required an external crystal or ceramic resonator. The clock circuit has now been integrated onto the device meaning that no crystal or ceramic resonator is required. However, if required, an external 12MHz crystal can be used as the clock source.

Integrated EEPROM - Previous generations of FTDI's USB to parallel FIFO interface devices required an external EEPROM if the device were to use USB Vendor ID (VID), Product ID (PID), serial number and product description strings other than the default values in the device itself. This external EEPROM has now been integrated onto the FT245R chip meaning that all designs have the option to change the product description strings. A user area of the internal EEPROM is available for storing additional data. The internal EEPROM is programmable in circuit, over USB without any additional voltage requirement.

Preprogrammed EEPROM - The FT245R is supplied with its internal EEPROM preprogrammed with a serial number which is unique to each individual device. This, in most cases, will remove the need to program the device EEPROM.

Integrated USB Resistors - Previous generations of FTDI's USB to parallel FIFO interface devices required two external series resistors on the USBDP and USBDM lines, and a 1.5 kΩ pull up resistor on USBDP. These three resistors have now been integrated onto the device.

Integrated AVCC Filtering - Previous generations of FTDI's USB to parallel FIFO interface devices had a separate AVCC pin - the supply to the internal PLL. This pin required an external R-C filter. The separate AVCC pin is now connected internally to VCC, and the filter has now been integrated onto the chip.

Less External Components - Integration of the crystal, EEPROM, USB resistors, and AVCC filter will substantially reduce the bill of materials cost for USB interface designs using the FT245R compared to its FT245BM predecessor.

Enhanced Asynchronous Bit Bang Mode with RD# and WR# Strobes - The FT245R supports FTDI's BM chip bit bang mode. In bit bang mode, the eight parallel FIFO data bus lines can be switched from the regular interface mode to an 8-bit general purpose I/O port. Data packets can be sent to the device and they will be sequentially sent to the interface at a rate controlled by an internal timer (equivalent to the baud rate prescaler). With the FT245R device this mode has been enhanced so that the internal RD# and WR# strobes are now brought out of the device which can be used to allow external logic to be clocked by accesses to the bit bang I/O bus. This option will be described more fully in a separate application note

Synchronous Bit Bang Mode - Synchronous bit bang mode differs from asynchronous bit bang mode in that the interface pins are only read when the device is written to. Thus making it easier for the controlling program to measure the response to an output stimulus as the data returned is synchronous to the output data. The feature was previously seen in FTDI's FT2232C device. This option will be described more fully in a separate application note.

Lower Supply Voltage - Previous generations of the chip required 5V supply on the VCC pin. The FT245R will work with a Vcc supply in the range 3.3V - 5V. Bus powered designs would still take their supply from the 5V on the USB bus, but for self powered designs where only 3.3V is available, and there is no 5V supply, there is no longer any need for an additional external regulator.

Integrated Level Converter on FIFO Interface and Control Signals - VCCIO pin supply can be from 1.8V to 5V. Connecting the VCCIO pin to 1.8V, 2.8V, or 3.3V allows the device to directly interface to 1.8V, 2.8V or 3.3V and other logic families without the need for external level converter I.C.s

5V / 3.3V / 2.8V / 1.8V Logic Interface - The FT245R provides *true* CMOS Drive Outputs and TTL level Inputs.

Integrated Power-On-Reset (POR) Circuit- The device incorporates an internal POR function. A RESET# pin is available in order to allow external logic to reset the FT245R where required. However, for many applications the RESET# pin can be left unconnected, or pulled up to VCCIO.

Wake Up Function - If USB is in suspend mode, and remote wake up has been enabled in the internal EEPROM (it is enabled by default), the RXF# pin becomes an input. Strobing this pin low will cause the FT245R to request a resume from suspend on the USB bus. Normally this can be used to wake up the host PC from suspend

Lower Operating and Suspend Current - The device operating supply current has been further reduced to 15mA, and the suspend current has been reduced to around 70µA. This allows a greater margin for peripherals to meet the USB suspend current limit of 500µA.

Low USB Bandwidth Consumption - The operation of the USB interface to the FT245R has been designed to use as little as possible of the total USB bandwidth available from the USB host controller.

High Output Drive Option - The parallel FIFO interface and the four FIFO handshake pins can be made to drive out at three times the standard signal drive level thus allowing multiple devices to be driven, or devices that require a greater signal drive strength to be interfaced to the FT245R. This option is configured in the internal EEPROM.

Power Management Control for USB Bus Powered, High Current Designs- The PWREN# signal can be used to directly drive a transistor or P-Channel MOSFET in applications where power switching of external circuitry is required. An option in the internal EEPROM makes the device gently pull down on its FIFO interface lines when the power is shut off (PWREN# is high). In this mode any residual voltage on external circuitry is bled to GND when power is removed, thus ensuring that external circuitry controlled by PWREN# resets reliably when power is restored.

FTDIChip-ID™ - Each FT245R is assigned a unique number which is burnt into the device at manufacture. This ID number cannot be reprogrammed by product manufacturers or end-users. This allows the possibility of using FT245R based dongles for software licensing. Further to this, a renewable license scheme can be implemented based on the FTDIChip-ID™ number when encrypted with other information. This encrypted number can be stored in the user area of the FT245R internal EEPROM, and can be decrypted, then compared with the protected FTDIChip-ID™ to verify that a license is valid. Web based applications can be used to maintain product licensing this way. An application note describing this feature is available separately from the FTDI website.

Improved EMI Performance - The reduced operating current and improved on-chip VCC decoupling significantly improves the ease of PCB design requirements in order to meet FCC, CE and other EMI related specifications.

Programmable FIFO TX Buffer Timeout - The FIFO TX buffer timeout is used to flush remaining data from the receive buffer. This timeout defaults to 16ms, but is programmable over USB in 1ms increments from 1ms to 255ms, thus allowing the device to be optimised for protocols that require fast response times from short data packets.

Extended Operating Temperature Range - The FT232R operates over an extended temperature range of -40º to +85º C thus allowing the device to be used in automotive and industrial applications.

New Package Options - The FT245R is available in two packages - a compact 28 pin SSOP (**FT245RL**) and an ultra-compact 5mm x 5mm pinless QFN-32 package (**FT245RQ**). Both packages are lead (Pb) free, and use a 'green' compound. Both packages are fully compliant with European Union directive 2002/95/EC.

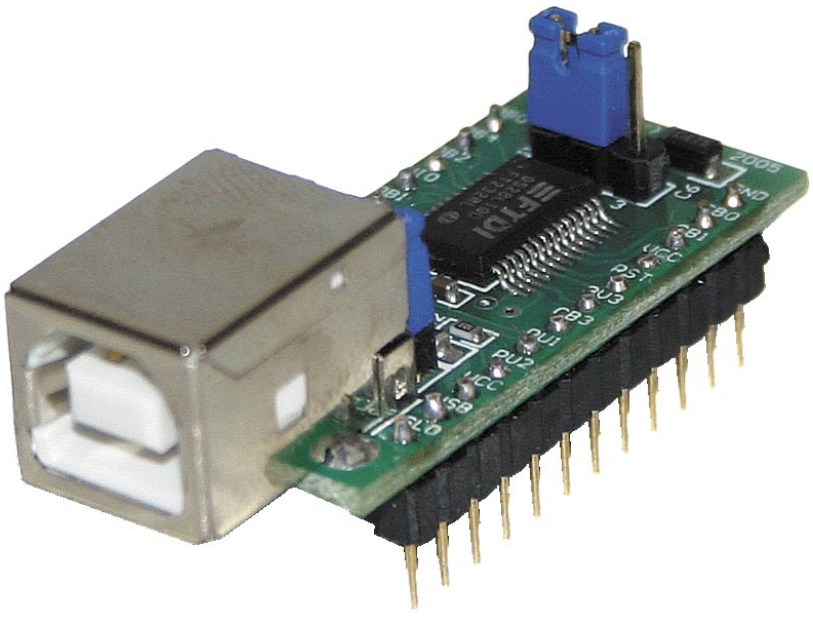


Figure 1 - UM245R Module

3. UM245R Pin Out and Signal Descriptions

3.1 UM245R Pin Out

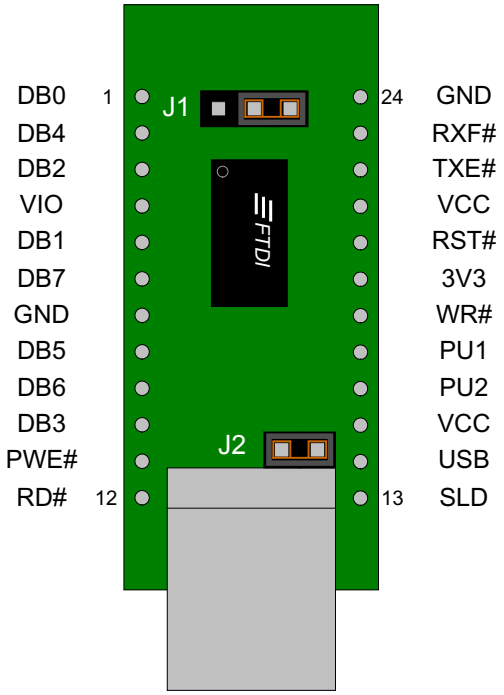


Figure 2 - Module Pin Out and Jumper Locations

3.2 UM245R Signal Descriptions

Table 1 - Module Pin Out Description

Pin No.	Name	Type	Description
1	DB0	I/O	FIFO Data Bus Bit 0*
2	DB4	I/O	FIFO Data Bus Bit 4*
3	DB2	I/O	FIFO Data Bus Bit 2*
4	VIO	PWR	+1.8V to +5.25V supply to the FIFO Interface and Control group pins (1...3, 5, 6, 9...14, 22, 23). In USB bus powered designs connect to 3V3OUT to drive out at 3.3V levels (connect jumper J1 pins 1 and 2 together), or connect to VCC to drive out at 5V CMOS level (connect jumper J1 pins 2 and 3 together). This pin can also be supplied with an external 1.8V - 2.8V supply in order to drive out at lower levels. It should be noted that in this case this supply should originate from the same source as the supply to Vcc. This means that in bus powered designs a regulator which is supplied by the 5V on the USB bus should be used.
5	DB5	I/O	FIFO Data Bus Bit 1*
6	DB7	I/O	FIFO Data Bus Bit 7*
7, 24	GND	PWR	Module ground supply pins
8	DB5	I/O	FIFO Data Bus Bit 5*
9	DB6	I/O	FIFO Data Bus Bit 6*
10	DB3	I/O	FIFO Data Bus Bit 3*
11	PWE#	I/O	Goes low after the device is configured by USB, then high during USB suspend. Can be used to control power to external logic P-Channel logic level MOSFET switch. Enable the interface pull-down option when using the PWREN# pin in this way.
12	RD#	I/O	Enables the current FIFO data byte on D0...D7 when low. Fetched the next FIFO data byte (if available) from the receive FIFO buffer when RD# goes from high to low. See Section 3.3 for timing diagram.*
13	SLD	GND	USB Cable shield.
14	USB	Output	5V Power output USB port. For a low power USB bus powered design, up to 100mA can be sourced from the 5V supply on the USB bus. A maximum of 500mA can be sourced from the USB bus in a high power USB bus powered design.
15, 21	VCC	PWR Input or Output	These pins are internally connected on the module pcb. To power the module from the 5V supply on USB bus connect jumper J2 pins 1 and 2 together (this is the module default configuration). In this case these pins would have the same description as pin 14. To use the UM245R module in a self powered configuration ensure that jumper J2 pins 1 and 2 are not connected together, and apply an external 3.3V to 5.25V supply to one or both of these pins.
16	PU1	Control	Pull up resistor pin connection 1. Connect to pin 14 (USB) in a self powered configuration
17	PU2	Control	Pull up resistor pin connection 2. Conect to pin 17 (RST#) in a self powered configuration.
19	3V3	Output	3.3V output from integrated L.D.O. regulator. This pin is decoupled to ground on the module pcb with a 10nF capacitor. The prime purpose of this pin is to provide the internal 3.3V supply to the USB transceiver cell and the internal 1.5kΩ pull up resistor on USBDP. Up to 50mA can be drawn from this pin to power external logic if required. This pin can also be used to supply the FT245RL's VCCIO pin by connecting this pin to pin 4 (VIO), or by connecting together pins 1 and 2 on jumper J1.
20	RST#	Input	Can be used by an external device to reset the FT245R. If not required can be left unconnected, or pulled up to VCCIO.
18	WR	I/O	Writes the data byte on the D0...D7 pins into the transmit FIFO buffer when WR goes from high to low. See Section 3.3 for timing diagram.*
22	TXE#	I/O	When high, do not write data into the FIFO. When low, data can be written into the FIFO by strobing WR high, then low. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 3.3 for timing diagram.
23	RXF#	I/O	When high, do not read data from the FIFO. When low, there is data available in the FIFO which can be read by strobing RD# low, then high again. During reset this signal pin is tri-state, but pulled up to VCCIO via an internal 200kΩ resistor. See Section 4.3 for timing diagram. If the Remote Wakeup option is enabled in the internal EEPROM, during USB suspend mode (PWREN# = 1) RXF# becomes an input which can be used to wake up the USB host from suspend mode. Strobing the pin low will cause the device to request a resume on the USB bus.

* When used in Input Mode, these pins are pulled to VCCIO via internal 200kΩ resistors. These can be programmed to gently pull low during USB suspend (PWREN# = "1") by setting this option in the internal EEPROM.

3.3 FT245R FIFO Control Interface Timing Diagrams

Figure 3 - FIFO Read Cycle

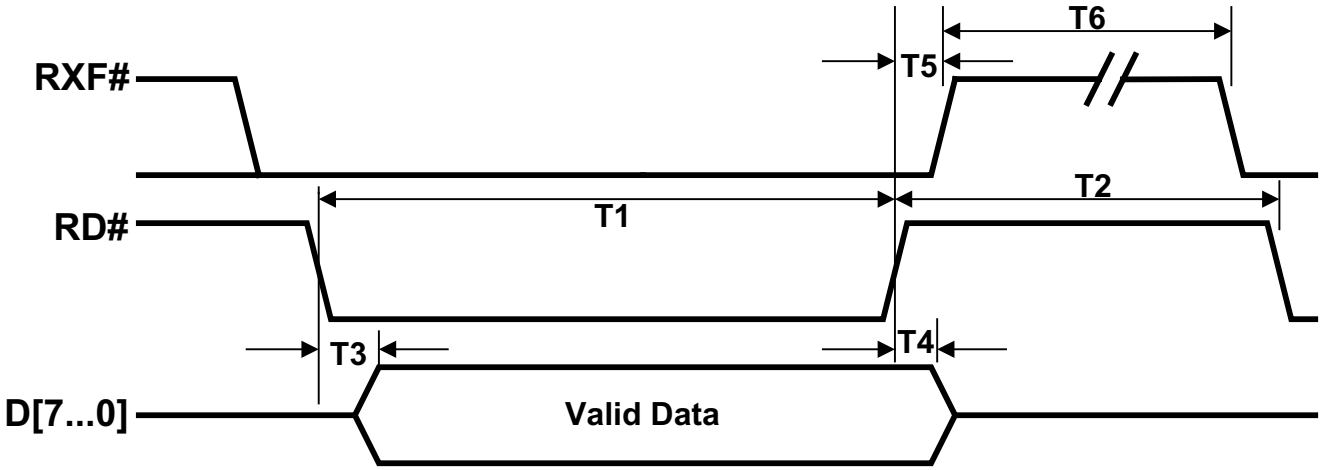


Table 2 - FIFO Read Cycle Timings

Time	Description	Min	Max	Unit
T1	RD Active Pulse Width	50		ns
T2	RD to RD Pre-Charge Time	50 + T6		ns
T3	RD Active to Valid Data*	20	50	ns
T4	Valid Data Hold Time from RD Inactive*	0		ns
T5	RD Inactive to RXF#	0	25	ns
T6	RXF Inactive After RD Cycle	80		ns

* Load = 30pF

Figure 4 - FIFO Write Cycle

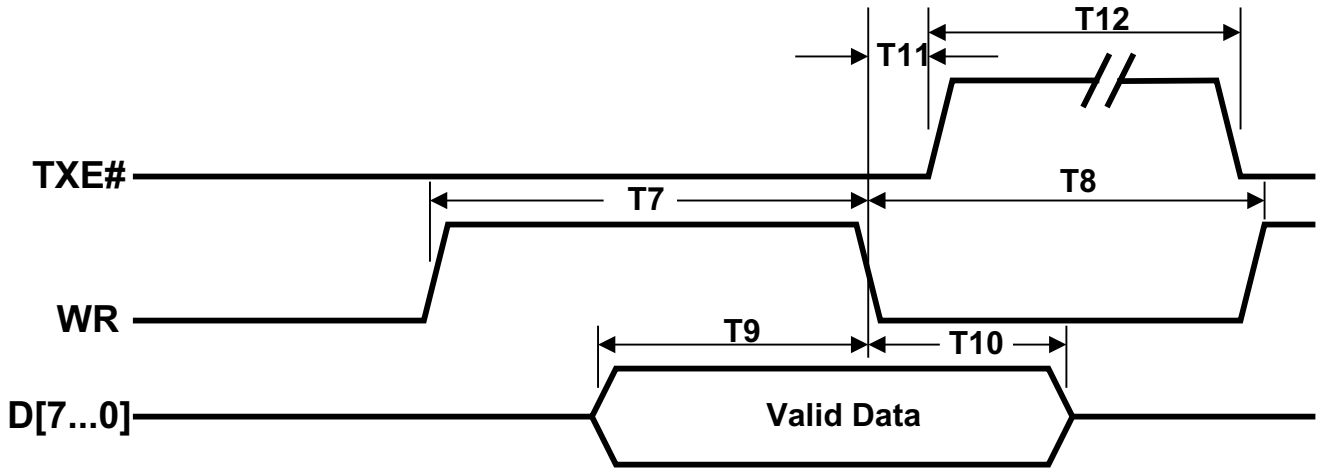
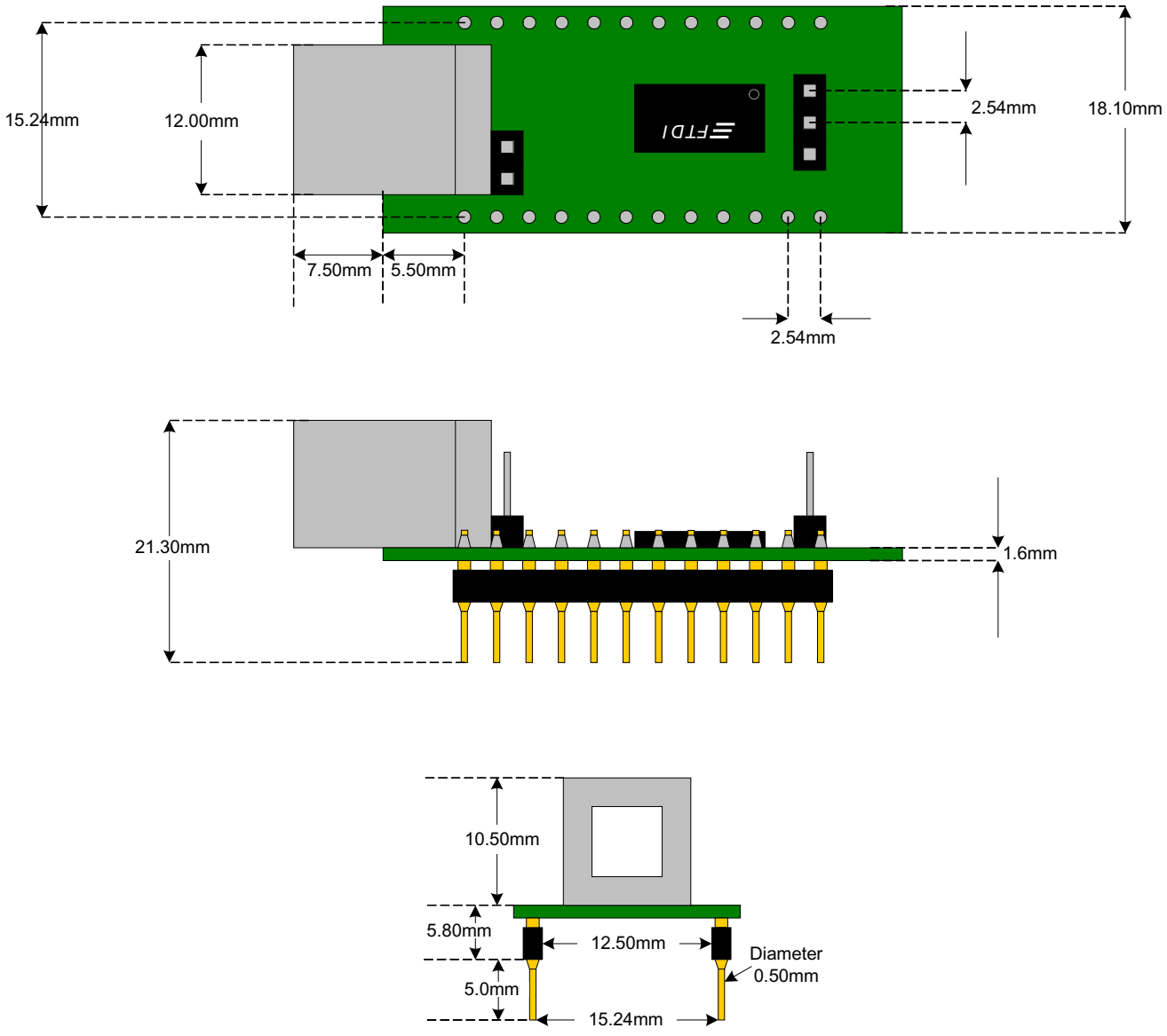


Table 3 - FIFO Write Cycle Timings

Time	Description	Min	Max	Unit
T7	WR Active Pulse Width	50		ns
T8	WR to RD Pre-Charge Time	50		ns
T9	Data Setup Time before WR Inactive	20		ns
T10	Data Hold Time from WR Inactive	0		ns
T11	WR Inactive to TXE#	5	25	ns
T12	TXE Inactive After WR Cycle	80		ns

4. UM245R Module Dimensions

Figure 4 - UM245R Module Dimensions



The FT245RL IC device used by the UM245R is supplied in a RoHS compliant 28 pin SSOP package. The package is lead (Pb) free and uses a 'green' compound. The date code format is **YYXX** where XX = 2 digit week number, YY = 2 digit year number.

The UM245R module uses exclusivly lead free components.

Both the I.C. device and the module are fully compliant with European Union directive 2002/95/EC.

5. Device Characteristics and Ratings

5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT245R devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these may cause permanent damage to the device.

Table 4 - Absolute Maximum Ratings

Parameter	Value	Unit
Storage Temperature	-65°C to 150°C	Degrees C
Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity)	168 Hours (IPC/JEDEC J-STD-033A MSL Level 3 Compliant)*	Hours
Ambient Temperature (Power Applied)	-40°C to 85°C	Degrees C.
Vcc Supply Voltage	-0.5 to +6.00	V
D.C. Input Voltage - USBDP and USBDM	-0.5 to +3.8	V
D.C. Input Voltage - High Impedance Bidirectionals	-0.5 to +(Vcc +0.5)	V
D.C. Input Voltage - All other Inputs	-0.5 to +(Vcc +0.5)	V
D.C. Output Current - Outputs	24	mA
DC Output Current - Low Impedance Bidirectionals	24	mA
Power Dissipation (Vcc = 5.25V)	500	mW

* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of 125°C and baked for up to 17 hours.

5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40 to 85°C)

Table 5 - Operating Voltage and Current

Parameter	Description	Min	Typ	Max	Units	Conditions
Vcc1	VCC Operating Supply Voltage	3.3	-	5.25	V	
Vcc2	VCCIO Operating Supply Voltage	1.8	-	5.25	V	
Icc1	Operating Supply Current	-	15	-	mA	Normal Operation
Icc2	Operating Supply Current	50	70	100	µA	USB Suspend*

*Supply current excludes the 200µA nominal drawn by the external pull-up resistor on USBDP.

Table 6 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 2mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 2mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 7 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.7	3.2	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 8 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, Standard Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.6	3.1	V	I source = 1mA
Vol	Output Voltage Low	0.3	0.4	0.5	V	I sink = 2 mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 9 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 5.0V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	3.2	4.1	4.9	V	I source = 6mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 6mA
Vin	Input Switching Threshold	1.3	1.6	1.9	V	**
VHys	Input Switching Hysteresis	50	55	60	mV	**

Table 10 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 3.3V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.2	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

Table 11 - FIFO Interface and Control Bus Pin Characteristics (VCCIO = 2.8V, High Drive Level)

Parameter	Description	Min	Typ	Max	Units	Conditions
Voh	Output Voltage High	2.1	2.8	3.2	V	I source = 3mA
Vol	Output Voltage Low	0.3	0.4	0.6	V	I sink = 8mA
Vin	Input Switching Threshold	1.0	1.2	1.5	V	**
VHys	Input Switching Hysteresis	20	25	30	mV	**

**Inputs have an internal 200kΩ pull-up resistor to VCCIO.

Table 12 - RESET#, TEST Pin Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
Vin	Input Switching Threshold	1.3	1.6	1.9	V	
VHys	Input Switching Hysteresis	50	55	60	mV	

Table 13 - USB I/O Pin (USBDP, USBDM) Characteristics

Parameter	Description	Min	Typ	Max	Units	Conditions
UVoh	I/O Pins Static Output (High)	2.8		3.6	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVol	I/O Pins Static Output (Low)	0		0.3	V	RI = 1.5kΩ to 3V3OUT (D+) RI = 15kΩ to GND (D-)
UVse	Single Ended Rx Threshold	0.8		2.0	V	
UCom	Differential Common Mode	0.8		2.5	V	
UVDif	Differential Input Sensitivity	0.2			V	
UDrvZ	Driver Output Impedance	26	29	44	Ohms	***

***Driver Output Impedance includes the internal USB series resistors on USBDP and USBDM pins.

5.3 EEPROM Reliability Characteristics

The internal 1024 Byte EEPROM has the following reliability characteristics-

Table 14 - EEPROM Characteristics

Parameter Description	Value	Unit
Data Retention	15	Years
Read / Write Cycles	100,000	Cycles

5.4 Internal Clock Characteristics

The internal Clock Oscillator has the following characteristics.

Table 15 - Internal Clock Characteristics

Parameter	Value			Unit
	Min	Typical	Max	
Frequency of Operation	11.98	12.00	12.02	MHz
Clock Period	83.19	83.33	83.47	ns
Duty Cycle	45	50	55	%

6. Module Configurations

6.1 Bus Powered Configuration

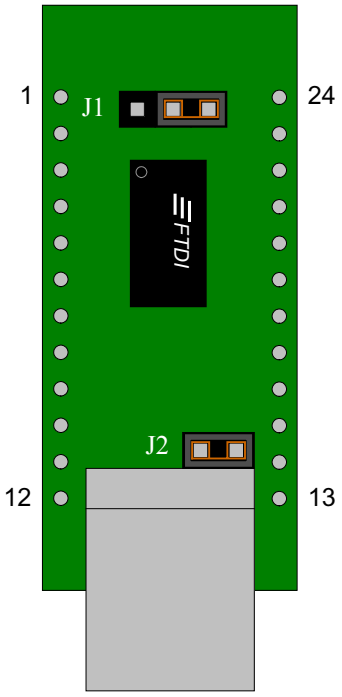


Figure 5 - Bus Powered Configuration

Figure 5 illustrates the UM245R in a typical USB bus powered design configuration. This can be done by fitting the jumper link on J2, as shown above. The UM245R is supplied in this configuration.

A USB Bus Powered device gets its power from the USB bus. Basic rules for USB Bus power devices are as follows –

i) On plug-in to USB, the device must draw no more than 100mA.

ii) On USB Suspend the device must draw no more than 500µA.

iii) A Bus Powered High Power USB Device (one that draws more than 100mA) should use the PWREN# pin to keep the current below 100mA on plug-in and 500µA on USB suspend.

iv) A device that consumes more than 100mA can not be plugged into a USB Bus Powered Hub.

v) No device can draw more that 500mA from the USB Bus.

See Figure 6 in Section 6.2 for an example of how to interface the UM245R module with a microcontroller. Interfacing this module to a microcontroller (or any other external logic) in a bus powered configuration would be exactly the same as in figure 6, except that the microcontroller would take its supply from the USB bus (i.e. either of the VCC pins or the USB pin).

Disclaimer

Copyright © Future Technology Devices International Limited , 2005.

Version 0.90 - Initial Datasheet Created December 2005
Version 0.91 - Revised Datasheet Released 6th December 2005

Neither the whole nor any part of the information contained in, or the product described in this manual, may be adapted or reproduced in any material or electronic form without the prior written consent of the copyright holder.

This product and its documentation are supplied on an as-is basis and no warranty as to their suitability for any particular purpose is either made or implied.

Future Technology Devices International Ltd. will not accept any claim for damages howsoever arising as a result of use or failure of this product. Your statutory rights are not affected.

This product or any variant of it is not intended for use in any medical appliance, device or system in which the failure of the product might reasonably be expected to result in personal injury.

This document provides preliminary information that may be subject to change without notice.

Contact FTDI

Head Office -

Future Technology Devices International Ltd.
373 Scotland Street,
Glasgow G5 8QB,
United Kingdom

Tel. : +(44) 141 429 2777
Fax. : +(44) 141 429 2758

E-Mail (Sales) : **sales1@ftdichip.com**
E-Mail (Support) : **support1@ftdichip.com**
E-Mail (General Enquiries) : **admin1@ftdichip.com**

Regional Sales Offices -

Future Technology Devices International Ltd. (Taiwan)
4F, No 16-1,
Sec. 6 Mincyuan East Road,
Neihu District,
Taipei 114,
Taiwan, R.o.C.

Tel.: +886 2 8791 3570
Fax: +886 2 8791 3576

E-Mail (Sales): **tw.sales@ftdichip.com**
E-Mail (Support): **tw.support@ftdichip.com**
E-Mail (General Enquiries): **tw.admin@ftdichip.com**

Future Technology Devices International Ltd. (USA)
5285 NE Elam Young
Parkway, Suite B800
Hillsboro,
OR 97124-6499
USA

Tel.: +1 (503) 547-0988
Fax: +1 (503) 547-0987

E-Mail (Sales): **us.sales@ftdichip.com**
E-Mail (Support): **us.support@ftdichip.com**
E-Mail (General Enquiries): **us.admin@ftdichip.com**

Website URL : **http://www.ftdichip.com**

