ACPL-M60L

High Speed LVTTL Compatible 3.3 Volt Optocouplers

Data Sheet

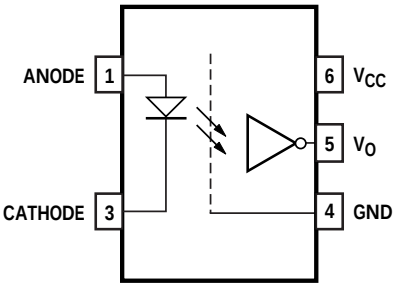
Description

The ACPL-M60L is an optically coupled gate that combines a GaAsP light emitting diode and an integrated high gain photo detector. The output of the detector IC is an open collector Schottky-clamped transistor. The internal shield provides a guaranteed common mode transient immunity specification of 15 kV/μs.

This unique design provides maximum AC and DC circuit isolation while achieving LVTTL/LVCMOS compatibility. The optocoupler AC and DC operational parameters are guaranteed from –40°C to +85°C, allowing trouble-free system performance.

These optocouplers are suitable for high speed logic interfacing, input/output buffering, as line receivers in environments that conventional line receivers cannot tolerate and are recommended for use in extremely high ground or induced noise environments.

Functional Diagram



Features

- **Low power consumption**
- **15 kV/μs minimum Common Mode Rejection (CMR) at V_{CM} = 1000 V**
- **High speed: 15 MBd typical**
- **LVTTL/LVCMOS compatible**
- **Low input current capability: 5 mA**
- **Guaranteed AC and DC performance over temperature: –40°C to +85°C**
- **Safety approvals; UL, CSA, IEC/EN/DIN EN 60747-5-2 (pending)**
- **Surface mountable**
- **Very small, low profile JEDEC Registered package outline**

Applications

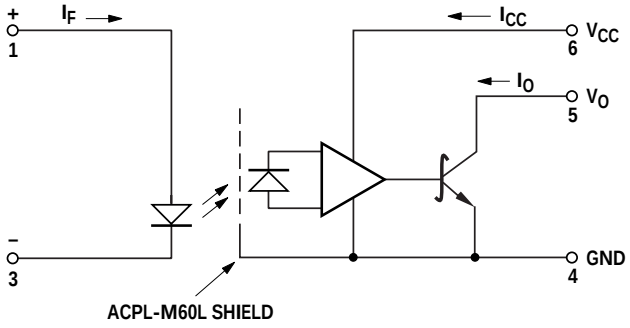
- **Isolated line receiver**
- **Computer-peripheral interfaces**
- **Microprocessor system interfaces**
- **Digital isolation for A/D, D/A conversion**
- **Switching power supply**
- **Instrument input/output isolation**
- **Ground loop elimination**
- **Pulse transformer replacement**
- **Field buses**

CAUTION: It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

Ordering Information

ACPL-M60L-000E (Tube package of 100 units, lead-free option)
ACPL-M60L-500E (Tape and Reel package of 1500 units, lead-free option)

Schematic

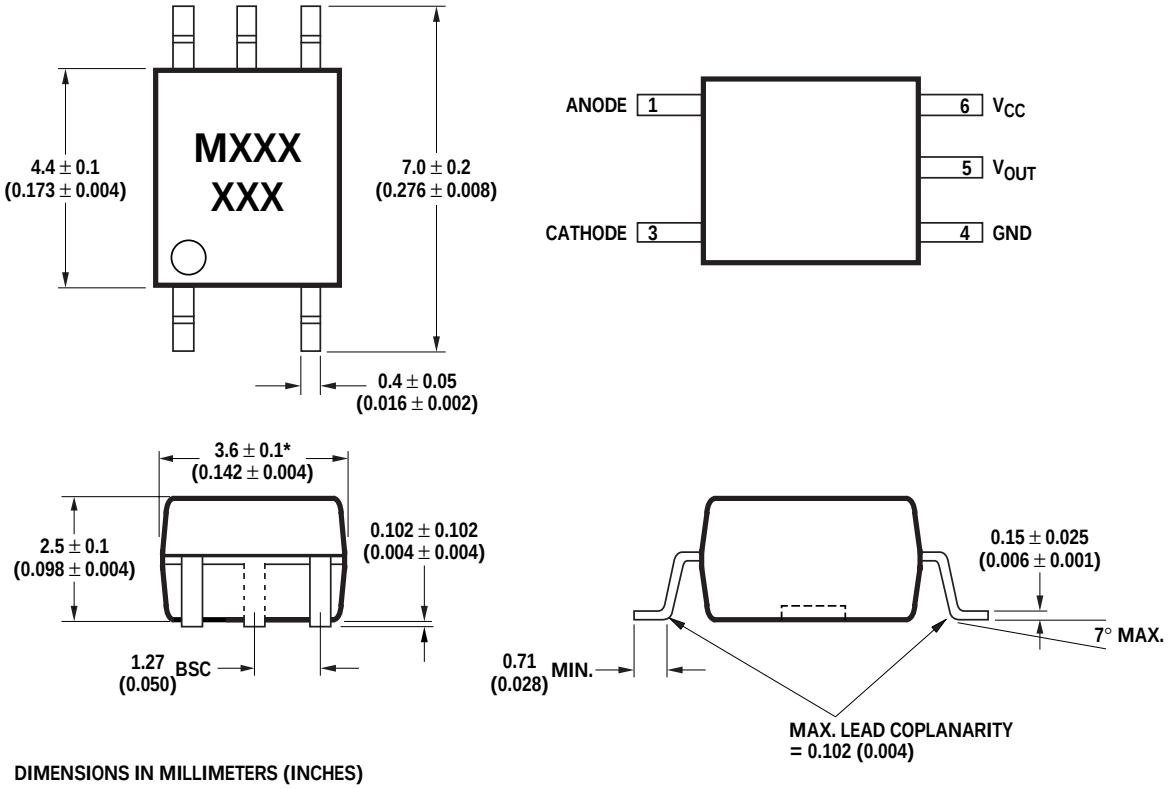


USE OF A 0.1 μF BYPASS CAPACITOR MUST BE CONNECTED BETWEEN PINS 6 AND 4 (SEE NOTE 1).

TRUTH TABLE (POSITIVE LOGIC)

LED	OUTPUT
ON	L
OFF	H

Package Outline Drawing

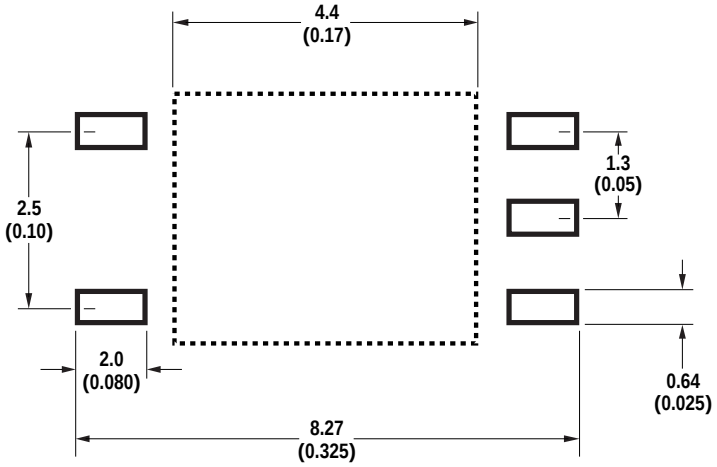


DIMENSIONS IN MILLIMETERS (INCHES)

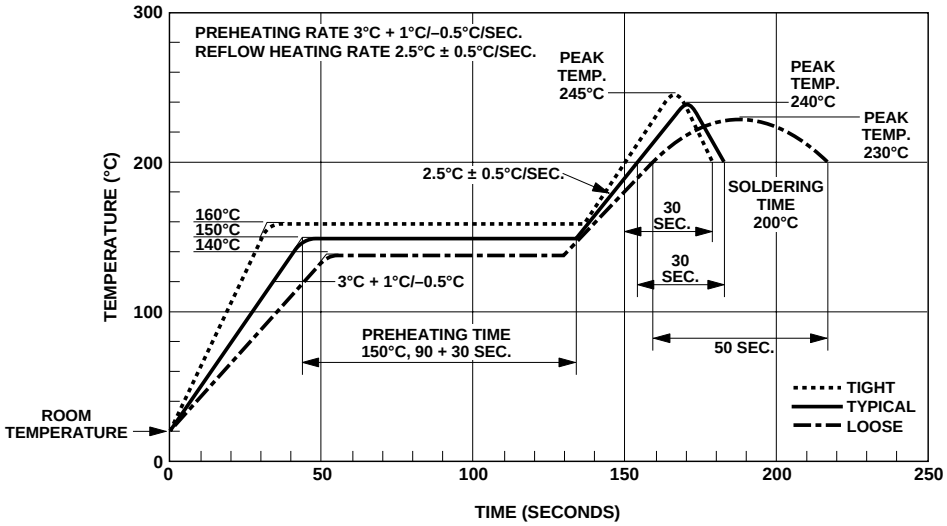
* MAXIMUM MOLD FLASH ON EACH SIDE IS 0.15 mm (0.006)

NOTE: FLOATING LEAD PROTRUSION IS 0.15 mm (6 mils) MAX.

Land Pattern

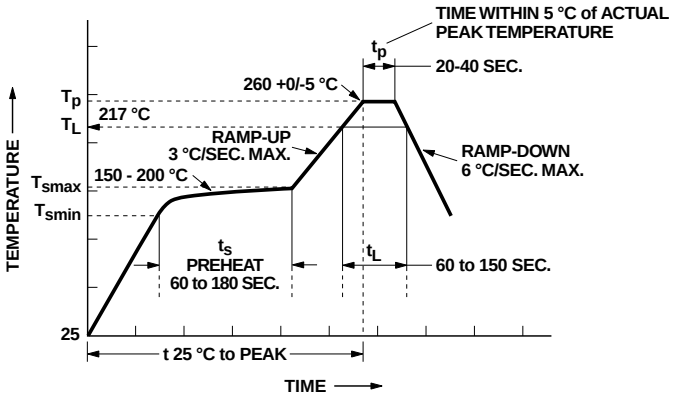


Solder Reflow Temperature Profile



Note: Use of non chlorine-activated fluxes is highly recommended.

Recommended PB-Free IR Profile



NOTES:
THE TIME FROM 25 °C to PEAK TEMPERATURE = 8 MINUTES MAX.
T_{smax} = 200 °C, T_{smin} = 150 °C

Note: Use of non chlorine-activated fluxes is highly recommended.

Insulation and Safety Related Specifications

Parameter	Symbol	Value	Units	Conditions
Minimum External Air Gap (Clearance)	L (I01)	≥ 5	mm	Measured from input terminals to output terminals
Minimum External Tracking Path (Creepage)	L (I02)	≥ 5	mm	Measured from input terminals to output terminals
Minimum Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance, conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Absolute Maximum Ratings (No Derating Required up to 85°C)

Parameter	Symbol	Min.	Max.	Units	Note
Storage Temperature	T_S	–55	125	°C	
Operating Temperature†	T_A	–40	85	°C	
Average Forward Input Current	I_F		20	mA	1
Reverse Input Voltage	V_R		5	V	
Input Power Dissipation	P_I		40	mW	
Supply Voltage (1 minute maximum)	V_{CC}		7	V	
Output Collector Current	I_O		50	mA	
Output Collector Voltage	V_O		7	V	
Output Collector Power Dissipation	P_O		85	mW	
Solder Reflow Temperature Profile		See Package Outline Drawings section			

Recommended Operating Conditions

Parameter	Symbol	Min.	Max.	Units
Input Current, Low Level	I_{FL}*	0	250	μA
Input Current, High Level[1]	I_{FH}**	5	15	mA
Power Supply Voltage	V_{CC}	2.7	3.6	V
Operating Temperature	T_A	–40	85	°C
Fan Out (at R_L = 1 kΩ)[1]	N		5	TTL Loads
Output Pull-up Resistor	R_L	330	4 k	Ω

*The off condition can also be guaranteed by ensuring that $V_{FL} \leq 0.8$ volts.
**The initial switching threshold is 5 mA or less. It is recommended that 6.3 mA to 10 mA be used for best performance and to permit at least a 20% LED degradation guardband.

Electrical Specifications

Over Recommended Temperature (T_A = –40°C to +85°C) unless otherwise specified.
All Typicals at V_{CC} = 3.3 V, T_A = 25°C.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
High Level Output Current	I_{OH}*		4.5	50	µA	V_{CC} = 3.3 V, V_O = 3.3 V, I_F = 250 µA	1	
Input Threshold Current	I_{TH}		3.0	5.0	mA	V_{CC} = 3.3 V, V_O = 0.6 V, I_{OL} (Sinking) = 13 mA	2	
Low Level Output Voltage	V_{OL}*		0.35	0.6	V	V_{CC} = 3.3 V, I_F = 5 mA, I_{OL} (Sinking) = 13 mA	3	
High Level Supply Current	I_{CCH}		4.7	7.0	mA	I_F = 0 mA V_{CC} = 3.3 V		
Low Level Supply Current	I_{CCL}		7.0	10.0	mA	I_F = 10 mA V_{CC} = 3.3 V		
Input Forward Voltage	V_F	1.4	1.5	1.75*	V	T_A = 25°C, I_F = 10 mA	5	
Input Reverse Breakdown Voltage	BV_R*	5			V	I_R = 10 µA		
Input Diode Temperature Coefficient	$\Delta V_F / \Delta T_A$		–1.6		mV°C	I_F = 10 mA		
Input Capacitance	C_{IN}		60		pF	f = 1 MHz, V_F = 0 V		

*The JEDEC Registration specifies 0°C to +70°C. Avago specifies –40°C to +85°C.

Switching Specifications

Over Recommended Temperature (T_A = –40°C to +85°C), V_{CC} = 3.3 V, I_F = 7.5 mA unless otherwise specified. All Typicals at T_A = 25°C, V_{CC} = 3.3 V.

Parameter	Sym.	Min.	Typ.	Max.	Units	Test Conditions	Fig.	Note
Propagation Delay Time to High Output Level	t_{PLH}			90	ns	R_L = 350 Ω C_L = 15 pF	6,7,8	5
Propagation Delay Time to Low Output Level	t_{PHL}			75	ns			6
Pulse Width Distortion	$\lvert t_{PHL} - t_{PLH} \rvert$			25	ns		8	8
Propagation Delay Skew	t_{PSK}			40	ns			
Output Rise Time (10-90%)	t_r		45		ns			
Output Fall Time (90-10%)	t_f		20		ns			

*JEDEC registered data for the 6N137.

Parameter	Sym.	Device	Min.	Typ.	Units	Test Conditions		Fig.	Note
Logic High Common Mode Transient Immunity	$\lvert CM_H \rvert$	ACPL-M60L	15,000	25,000	V/µs	$\lvert V_{CM} \rvert$ = 1000 V	V_{CC} = 3.3 V, I_F = 0 mA, $V_{O(MIN)}$ = 2 V, R_L = 350 Ω, T_A = 25°C	9	9, 11
Logic Low Common Mode Transient Immunity	$\lvert CM_L \rvert$	ACPL-M60L	15,000	25,000	V/µs	$\lvert V_{CM} \rvert$ = 1000 V	V_{CC} = 3.3 V, I_F = 7.5 mA, $V_{O(MAX)}$ = 0.8 V, R_L = 350 Ω, T_A = 25°C	9	10, 11

Notes:

1. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 20 mA.
2. Peaking circuits may produce transient input currents up to 50 mA, 50 ns maximum pulse width, provided average current does not exceed 15 mA.
3. Derate linearly above +80°C free-air temperature at a rate of 2.7 mW/°C for the SOIC-8 package.
4. Bypassing of the power supply line is required, with a 0.1 µF ceramic disc capacitor adjacent to each optocoupler. Total lead length between both ends of the capacitor and the isolator pins should not exceed 20 mm.
5. The t_{PLH} propagation delay is measured from the 3.75 mA point on the falling edge of the input pulse to the 1.5 V point on the rising edge of the output pulse.
6. The t_{PHL} propagation delay is measured from the 3.75 mA point on the rising edge of the input pulse to the 1.5 V point on the falling edge of the output pulse.
7. t_{PSK} is equal to the worst case difference in t_{PHL} and/or t_{PLH} that will be seen between units at any given temperature and specified test conditions.
8. See test circuit for measurement details.
9. CM_H is the maximum tolerable rate of rise on the common mode voltage to assure that the output will remain in a high logic state (i.e., V_o > 2.0 V).
10. CM_L is the maximum tolerable rate of fall of the common mode voltage to assure that the output will remain in a low logic state (i.e., V_o < 0.8 V).
11. For sinusoidal voltages, $(\lvert dV_{CM} \rvert / dt)_{max} = \pi f_{CM} V_{CM}$ (p-p).

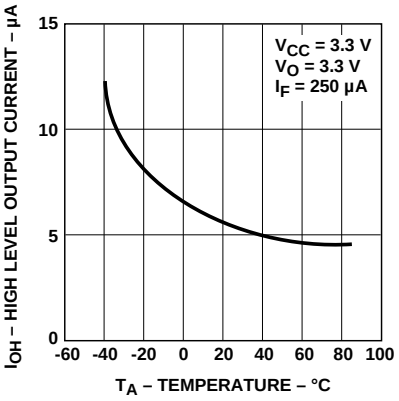


Figure 1. Typical high level output current vs. temperature.

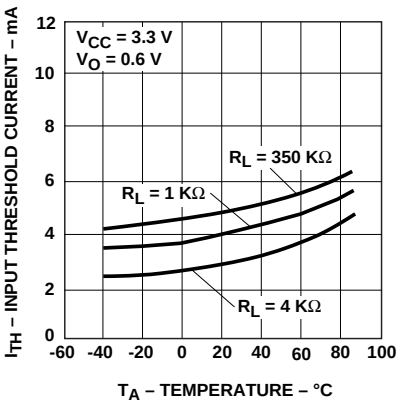


Figure 2. Typical input threshold current vs. temperature.

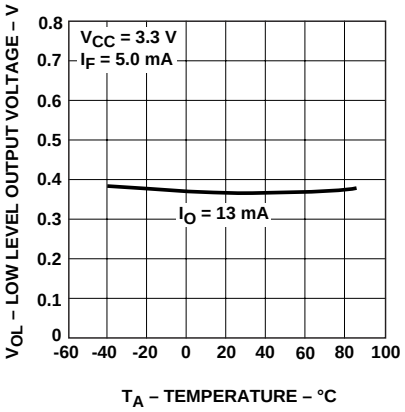


Figure 3. Typical low level output voltage vs. temperature.

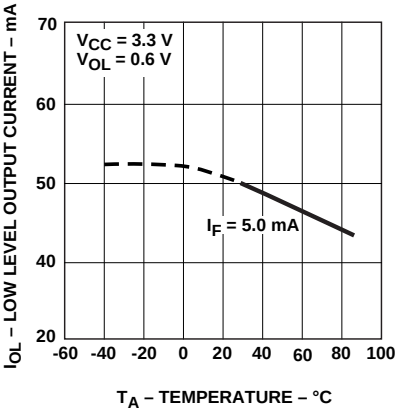


Figure 4. Typical low level output current vs. temperature.

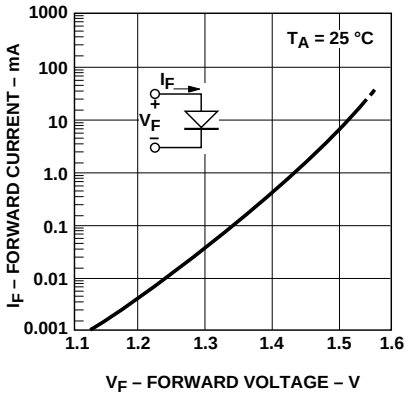


Figure 5. Typical input diode forward characteristic.

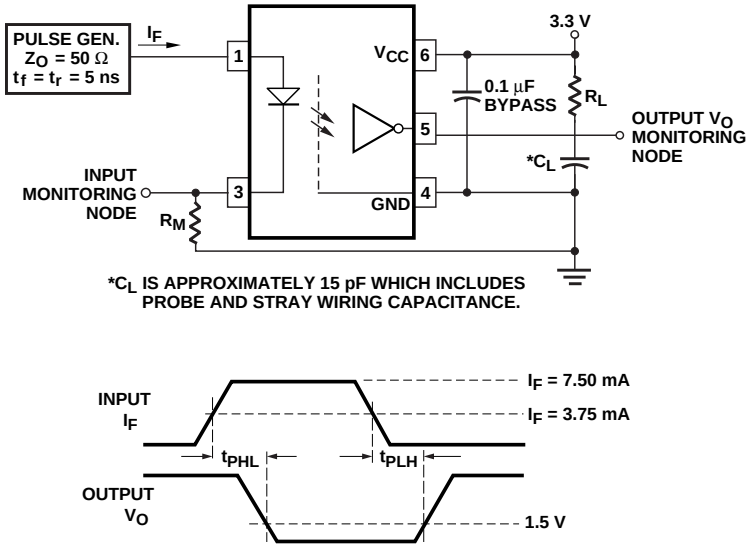


Figure 6. Test circuit for t_{PHL} and t_{PLH}.

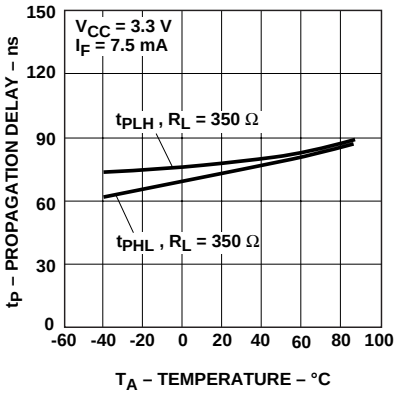


Figure 7. Typical propagation delay vs. temperature.

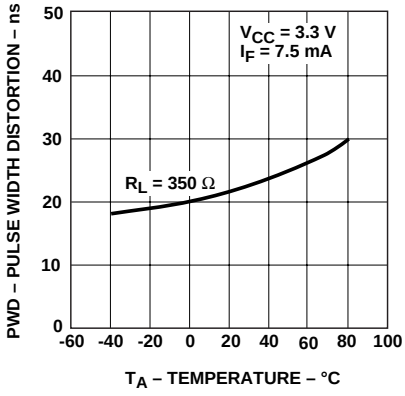
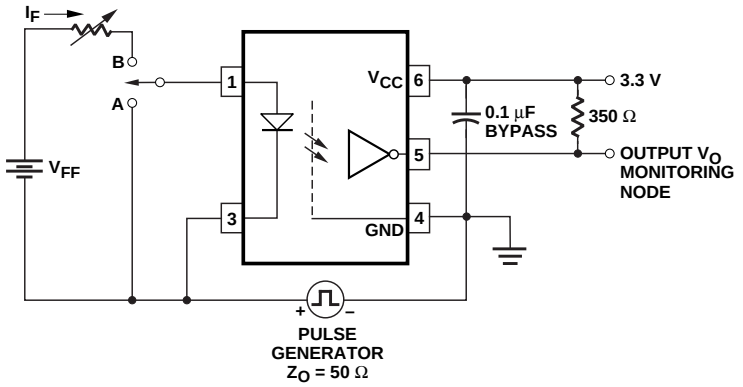


Figure 8. Typical pulse width distortion vs. temperature.



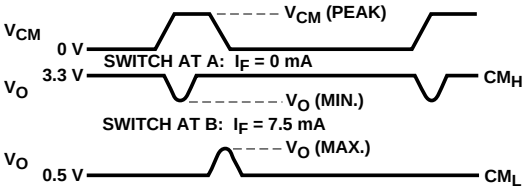


Figure 9. Test circuit for common mode transient immunity and typical waveforms.

For product information and a complete list of distributors, please go to our website: **www.avagotech.com**

AV01-0273EN June 26, 2006